AMPP Catalog
February 1997

About this Catalog

February 1997

AMPP Catalog Contents

This catalog describes the Altera® Megafunction Partners Program (AMPP). The catalog also provides megafunction descriptions and partner profiles for each AMPP partner. The information in this catalog is current as of the print date, but megafunction specifications and availability are subject to change. For the most current information, refer to the Altera world-wide web site at **http://www.altera.com**.

Each megafunction description includes a list of key features, a functional description with information on applicable standards compliance, and a table with fitting and performance specifications. See page 11 for more details.

Table 2 on page 11 lists and categorizes all the megafunctions in this catalog into one or more of the following application areas

- Buses and Interfaces
- Processors and Peripherals
- Telecommunications and Data Communications (Telecom & Datacom)
- DSP for Imaging
- DSP for Communications

Each AMPP partner profile contains contact, background, and historical information on the partner company. The partner profile may also include a list of available megafunctions and a description of additional services. Not all megafunctions from all AMPP partners are available for Altera device architectures. If a megafunction appears in a partner profile but does not have a corresponding megafunction description, contact the AMPP partner directly for information on availability.

For additional details on megafunctions, including availability, pricing, and delivery terms, designers should contact the AMPP partner directly.

How to Contact Altera

For additional information about Altera products, consult the sources shown in Table 1. For information on how to contact an Altera sales office, see "Altera Sales Offices" in this catalog.

Table 1. Contact Information

Information Type	Access	U.S. & Canada	All Other Locations
Literature	Altera Express	(800) 5-ALTERA	(408) 894-7850
	Altera Literature Services	(888) 3-ALTERA lit_req@altera.com	(888) 3-ALTERA lit_req@altera.com
Non-Technical Customer Service	Telephone Hotline	(800) SOS-EPLD	(408) 894-7000
	Fax	(408) 954-8186	(408) 954-8186
Technical Support	Telephone Hotline (8 a.m. to 5 p.m. PST)	(800) 800-EPLD	(408) 894-7000
	Fax	(408) 954-0348	(408) 954-0348
	Bulletin Board Service	(408) 954-0104	(408) 954-0104
	Electronic Mail	sos@altera.com	sos@altera.com
	FTP Site	ftp.altera.com	ftp.altera.com
	CompuServe	go altera	go altera
General Product Information	Telephone	(408) 894-7104	(408) 894-7104
	World-Wide Web	http://www.altera.com	http://www.altera.com

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Section 2: Megafunction Descriptions *(Continued)*

Section 3: AMPP Partner Profiles *(Continued)*

Introduction

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Overview

As programmable logic device (PLD) density continues to increase, Altera recognizes that designers require design tools that will increase their productivity and allow them to keep pace with the increasing capacity of PLDs. A design methodology that uses pre-built megafunctions offers this productivity increase. The successful development of megafunctions requires close cooperation between the intellectual property (IP) developers and PLD vendors. The Altera Megafunction Partners Program (AMPP), established in August 1995, was created to bring the advantages of megafunctions to users of Altera PLDs.

AMPP identifies megafunction developers, trains them on the Altera device architectures and tools, and promotes the partners' megafunctions through Altera's broad marketing and sales channel. Altera does not participate in the licensing or delivery of AMPP megafunctions; the actual delivery and licensing of megafunctions is between the designer and the AMPP partner.

Altera carefully selects each AMPP partner; continuing participation in AMPP is subject to the partner's active involvement in developing new megafunctions. By recruiting a diverse group of participants, Altera hopes to provide the widest range of megafunctions while minimizing product overlaps. An AMPP partner must meet at least two criteria:

- Be large enough to handle Altera's world-wide business
- Have a roadmap of future megafunction products

AMPP partners are required to attend training sessions provided by Altera, and are encouraged to re-attend future training sessions. Partners are instructed on how to develop megafunctions and to support the encrypted megafunctions in the field.

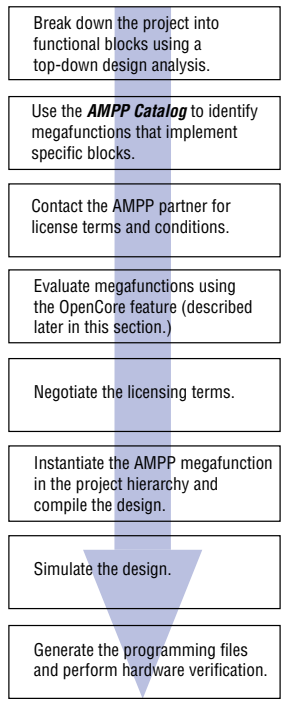
AMPP partners and the Altera sales staff work closely together to establish relationships with customers and to provide timely resources during megafunction evaluation and implementation.

About AMPP Megafunctions

AMPP megafunctions are optimized for specific Altera device architectures. The optimization process usually involves setting compilation and synthesis options to maximize density and performance. AMPP megafunctions are then refined until they are as fast and small as possible.

Figure 1 illustrates the typical process for evaluating, licensing, and using AMPP megafunctions.

Figure 1. Using AMPP Megafunctions



The AMPP megafunctions can be parameterized, programmed, and/or customized. Parameterizable megafunctions can be changed during design processing by setting options in the MAX+PLUS® II software. Programmable megafunctions can be configured "on-the-fly," which changes behavior or specific function settings (e.g., a shift register with a dynamically adjustable maximum depth). Customizable megafunctions are modified by AMPP partners to create new versions. Megafunctions that are customized may be included in the quoted license fee, but are typically subject to additional modification/consulting fees.

Available Megafunctions

Table 2 lists the AMPP megafunctions and their applications. In this table, megafunctions with similar industry-standard numbers are listed together (e.g., the RAW8051-A, RAW8052-A, and BareCore 8052 are listed together in numeric sequence).

Table 2. AMPP Megafunction Applications (Part 1 of 2)

Megafunction	AMPP Partner	Buses & Interfaces	Processors & Peripherals	Telecom & Datacom	DSP for Imaging	DSP for Communications	Page
IEEE 1284 Parallel Slave Interface	SIS	✓	✓				12
C2910 Microprogram Controller	CAST		✓				13
C49410 Microprogram Controller	CAST		✓				14
V6502 Microprocessor	VAutomation		✓				15
C68450 DMA Controller	CAST		✓				16
C6850 ACIA	CAST		✓	✓			17
VZ80 Microprocessor	VAutomation		✓				19
C8051 Microcontroller	CAST		✓				20
RAW8051-A	RWA		✓				21
RAW8052-A	RWA		✓				22
BareCore 8052	RWA		✓				23
C8255 Peripheral Interface	CAST		✓				24
Adaptive Filters	ISS				✓	✓	25
Binary Pattern Correlator	Nova					✓	26
Biorthogonal Wavelet Filter	FASTMAN				✓		27
C_UART	CAST		✓	✓			28
Complex Multiplier/Mixer	Nova					✓	29
Convolutional Interleaver	KTech					✓	30
Decimating Filter	FASTMAN				✓	✓	31
Digital Modulator	Nova					✓	32
Discrete Cosine Transform	ISS				✓		33
Early/Late-Gate Symbol Synchronizer	Nova					✓	34
FIR Filter Library	ISS				✓	✓	35
Floating-Point Adder	ISS				✓	✓	36

Table 2. AMPP Megafunction Applications (Part 2 of 2)

Megafunction	AMPP Partner	Buses & Interfaces	Processors & Peripherals	Telecom & Datacom	DSP for Imaging	DSP for Communications	Page
Floating-Point Divider	ISS				✓	✓	37
Floating-Point Multiplier	ISS				✓	✓	38
HDLC	ISS			✓			39
IIR Filter Library	ISS				✓	✓	40
Image Processing Library	ISS				✓		41
Integer Divider	ISS				✓	✓	42
JPEG Decoder and Encoder	ISS				✓		43
JPEG Decoder and Encoder	Synova				✓		44
Linear Feedback Shift Register	Nova					✓	46
Median Filter Library	ISS				✓	✓	47
Multi-Standard ADPCM	ISS					✓	45
Numerically Controlled Oscillator	Nova					✓	48
PCI Bus Master (EC200)	Eureka	✓					49
32-Bit PCI Bus M/T	Logic Innovations	✓					50
PCI Bus Target (EC100)	Eureka	✓					51
PowerPC Bus Arbiter (EP300)	Eureka	✓	✓				52
PowerPC Bus Master (EP200)	Eureka	✓	✓				53
PowerPC Bus Slave (EP100)	Eureka	✓	✓				54
Rank Order Filter Library	ISS				✓	✓	55
Reed-Solomon Decoder	ISS			✓		✓	56
Reed-Solomon Encoder	ISS			✓		✓	57
Speedbridge	SIS			✓			59
Square Root Operator	ISS				✓	✓	60
XMIDI Modules UART Library	DDD	✓					60
XM-01 XMIDI Basic UART	DDD	✓					60

Available Formats

All AMPP megafunctions are available in post-synthesis AHDL format, a fully minimized and optimized netlist that can be used without risk of changes during design processing. Although VHDL and Verilog HDL files are available from most partners, a source code license is usually more expensive than a post-synthesis netlist license because the source code versions represent more intrinsic value.

Altera recommends using post-synthesis netlists to avoid synthesis variation issues during design processing. This process ensures that no engineering effort is required to reoptimize the behavioral source code.

OpenCore Feature

Altera's MAX+PLUS II software provides the OpenCore feature, which allows the designer to evaluate the megafunction prior to purchasing the license. OpenCore allows the designer to compile the megafunction and determine the megafunction's size and speed, but it prevents the designer from generating programming files. This feature allows AMPP partners to offer OpenCore evaluations without risking their licensing interests.

Megafunctions in the Design Flow

AMPP megafunctions are intended as "drop-in" design elements for all design flows supported by MAX+PLUS II. Although the megafunctions are developed as stand-alone functions, they can be integrated with other megafunctions and logic in a top-down design methodology. The ideal design flow assesses a project's functional block requirements and assigns megafunctions to implement different portions of a system. Once the megafunction blocks are defined, designers can focus on design elements that cannot be sourced as megafunctions or that are proprietary features of the system.

AMPP megafunction support extends to third-party design flows that are currently supported by Altera tools. For design flows that use standard EDA tools, designers can instantiate AMPP megafunctions in a design by specifying the cell and port names in an HDL design file. For design flows that are entirely within MAX+PLUS II, the designer can use the megafunction in a Graphic Design File (**.gdf**), AHDL Text Design File (**.tdf**), or VHDL Design File (**.vhd**).

During design processing, the EDA tool will pass the megafunction's cell and port names into the EDIF file. Assuming that some downstream processing tool will replace the cell name with the actual functional specification, the EDA tool will not process beyond the name level. Once the megafunction is part of a MAX+PLUS II project hierarchy, the designer must specify three synthesis options before the megafunction is processed by MAX+PLUS II:

- Assign the megafunction to a clique, which ensures that the placement of the megafunction is optimized for high performance.
- Assign the WYSIWYG logic synthesis style, which tells the MAX+PLUS II software to turn off logic synthesis when it processes the megafunction.
- Apply any top-level timing assignments provided by the AMPP partner to the hierarchy before design processing.

For information on cliques, logic synthesis styles, and instantiating functions, go to MAX+PLUS II Help.

During compilation, MAX+PLUS II recognizes the megafunction as an AMPP megafunction and verifies that there is a valid megafunction license. MAX+PLUS II then completes design processing according to the permissions granted by the AMPP megafunction license.

Performance & Density Specifications

The performance and density specifications in this catalog apply to megafunctions that are compiled as stand-alone designs. Additional logic synthesis may affect the performance or density of a megafunction, particularly when the function is combined with other megafunctions or logic. Megafunctions shipped as post-synthesis AHDL files have minimal performance or density variations, because additional design processing is not required. Megafunctions supplied as behavioral source code files may experience changes in performance or density, depending on the design and the target device. Timing cannot be determined until synthesis and placement of the final design is complete.

Each AMPP megafunction has a performance metric that provides performance information when the megafunction is compiled as a stand-alone project. The metric is usually a global clock speed or f_{MAX}, but in some cases, other metrics such as a propagation delay or sample/second is given. The global clock setup time (t_{SU}) and global clock-to-output (t_{CO}) delay are also useful parameters. Contact the AMPP partner to determine which performance metric is available for the megafunction.

In general, a global clock frequency is not affected by the I/O delays that route the signal off-chip, whereas the t_{SU} and t_{CO} parameters are directly impacted by on-chip and off-chip routing. If a megafunction is integrated with other logic or megafunctions on the same device, the set-up and clock-to-output delays will be reduced because off-chip/on-chip delays are not required.

Subsequent versions of MAX+PLUS II, megafunction design modifications, or the availability of faster speed-grade devices may affect density or performance characteristics. Contact the AMPP partners for the latest megafunction specifications.

AMPP Megafunction Package Contents

An AMPP megafunction package typically contains the following items (items that accompany every package are highlighted in blue):

- Megafunction license
- Megafunction design file (typically a post-synthesis netlist)
- Symbol File (**.sym**) for use in MAX+PLUS II GDFs
- Include File (**.inc**) for use in MAX+PLUS II TDFs
- VHDL and Verilog HDL instantiation templates
- Megafunction documentation
- Top-level timing assignments
- Help file (typically in HTML)
- Simulation stimulus file(s)

AMPP partners have different levels of support and documentation. Designers should contact the AMPP partner directly to ensure that appropriate support will be provided. Most partners will supply more sophisticated simulation information, such as pre-synthesis bus simulation models for use in third-party logic synthesis tools, prior to processing in MAX+PLUS II.

Licensing AMPP Megafunctions

AMPP megafunction are licensed directly from AMPP partners. The terms and conditions for the license of each AMPP megafunction may vary from partner to partner. Each AMPP partner typically specifies the megafunction licensing terms based on the needs of the end user. AMPP megafunction license options may include:

- Duration of the license (e.g., lifetime, 1 year, or 6 months)
- Source-code access
- OpenCore feature

AMPP megafunction licenses generally limit the use of the licensed AMPP megafunction to PLDs from Altera. Permission should be received in writing from the AMPP partner before an AMPP megafunction is used in a target device other than an Altera PLD (e.g., an MPLD from Altera, or a gate array). Such use of an AMPP megafunction may possibly require an additional license and/or fee payment to the AMPP partner.

The duration of an AMPP megafunction license typically defines the period of time during which the AMPP megafunction may be compiled as part of a project in MAX+PLUS II. Once the programming file for an Altera PLD has been created, AMPP megafunction licenses generally convey unlimited lifetime manufacturing rights to use the licensed megafunction in Altera PLDs as incorporated in the programming file. Any limitations in the use of the licensed megafunction may vary from partner to partner.

To protect the embedded intellectual property, AMPP megafunctions are typically shipped as encrypted files. Although the megafunction design file will have a standard filename (e.g., **function.tdf**), the file will appear corrupted when opened with a text editor. The encrypted megafunction design file is actually a binary file. Access authorization and decryption are handled by MAX+PLUS II, using a megafunction authorization code that is generated and supplied by the AMPP partner.

AMPP megafunction licenses use the same authorization process as the MAX+PLUS II software. PC/Windows installations of MAX+PLUS II use an embedded license system, based on the serial number of the MAX+PLUS II software guard (guard ID). Workstation installations of MAX+PLUS II use the FLEXlm license manager and treat each AMPP megafunction as a new MAX+PLUS II feature. Workstation licensing can either be locked or floating node, depending on the licensing partner's policy.

AMPP megafunctions licenses are supplied by the AMPP partners, not by Altera. Altera does not have the ability to generate any license for any AMPP megafunction.

AMPP Megafunction Pricing

Designers should contact the appropriate AMPP partner for a price quote or estimate on a megafunction license. To help determine the cost of a megafunction license and to ensure that the megafunction successfully integrates with the end application, be prepared to provide the AMPP partner with the following information:

- Relevant megafunction parameters (e.g., bus width, resolution)
- License duration requirements (e.g., lifetime, 6 months)
- Target device architecture (e.g., FLEX 10K, MAX 9000)
- Netlist-only or source-code license
- Any requirements for modifications or feature changes
- Any requirements for design migration (e.g., to a gate array or ASIC device)

Technical Support

AMPP megafunctions are carefully developed by AMPP partners to ensure the highest possible quality. If a problem is traced to a megafunction, the AMPP partner is responsible for resolving the problem.

If a problem arises with integrating the megafunction with other logic, Altera will provide appropriate engineering support.

Warranty

The megafunctions in this catalog, as well as other megafunctions and services available from the AMPP partners, are provided without warranty by Altera. Altera expressly disclaims all warranties, express and implied, with respect to the megafunctions supplied by the AMPP partners, including, but not limited to, implied warranties of merchantability, fitness for a particular purpose, title and non-infringement.

The AMPP partners may offer guarantees or warranties for design performance or functionality; contact the individual AMPP partners for details.

Megafunction Descriptions

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Overview

The megafunction descriptions provide highlighted features, typical applications, and general and functional descriptions for each AMPP megafunction. In the size and performance information tables, the following megafunction information are also provided:

- *Smallest target device*—Indicates the smallest device that can implement the megafunction as a stand-alone design. Adding other megafunctions or user-supplied logic may require a larger device.
- *Device utilization*—Shows the logic cells (LCs) required, and for the FLEX 10K family, the EABs used. If any partner-supplied usage guidelines are followed, the megafunction's device utilization should not change when the megafunction is integrated with other logic.
- *Performance*—Typically expressed as a maximum global clock frequency (f_{MAX}). When the megafunction is compiled with other logic, the maximum frequency may change. Other performance metrics are possible (e.g., samples/second or $\mathbf{t_{PD}}$), and will be indicated where applicable.
- *Availability*—Indicates when the megafunction is available (e.g., available now, Q2 1997). Contact the AMPP partner for the most current information on availability.

IEEE 1284 Parallel Slave Interface

SIS Microelectronics
See profile on page 67.

Applications

- ✓ Buses & Interfaces
- ✓ Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- Bidirectional interface between host computers and peripheral devices
- Uses standard parallel port found on many computer systems
- Fully tested, includes a complete test suite
- Configurable for compatible mode timing of nACK and BUSY ports
- Asserts interrupt or DMA request when the transmit buffer is empty or the receive buffer contains data

The IEEE 1284 bidirectional parallel slave interface megafunction is an interface for fully interlocked, asynchronous bidirectional parallel communications between host computers and peripherals.

The megafunction is compatible with the 8-bit IEEE 1284 and Centronics parallel printer port interfaces, and it can read data from and write data to the parallel printer port interface. The megafunction supports five operational modes: forward compatibility mode, ECP mode with forward-only RLE, ECP mode (forward and reverse), reverse nibble mode, and request device ID using nibble mode (reverse only).

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K	EPF10K30	-3	1,350	0	33 MHz	Available Now
FLEX 8000	EPF81500A	A-2	1,250	–	33 MHz	Available Now
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

C2910 Microprogram Controller

CAST
See profile on page 62.

Applications

- Buses & Interfaces
- ✓ Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- 12-bit data width that addresses up to 4,096 microcode words
- Internal loop counter
- 16 powerful microinstructions
- Four address sources
- Positive-edge-triggered registers

The C2910 microprogram controller megafunction is an address sequencer that controls the execution sequence of the microinstructions stored in the microprogram memory. The megafunction can sequentially access the microinstructions, and it provides conditional branching to any microinstructions within the 4,096-microword range. In addition, a five-deep LIFO stack provides a microsubroutine return linkage and looping capability.

The C2910 microprogram controller megafunction can be customized to a C2910A megafunction. Contact CAST for more information on customization.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K	EPF10K10	-3	240	0	22 MHz	Available Now
FLEX 8000, *Note (2)*	EPF8452A	A-3	291	–	23 MHz	Available Now
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) A smaller version of the megafunction that requires 237 LCs and operates at 14 MHz is also available.

C49410 Microprogram Controller

CAST
See profile on page 62.

Applications

- Buses & Interfaces
- ✓ Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- 16-bit data width that addresses up to 65,536 microcode words
- Internal loop counter
- 16 powerful microinstructions
- Four address sources
- Positive-edge-triggered registers

The C49410 microprogram controller megafunction is an address sequencer that controls the execution sequence of the microinstructions stored in the microprogram memory. The megafunction sequentially accesses the microinstructions, and it provides conditional branching to any microinstructions within the 65,536-microword range. In addition, a 33-deep LIFO stack provides a microsubroutine return linkage and looping capability.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K	EPF10K20	-3	1,218	0	16 MHz	Available Now
FLEX 8000	EPF81500A	A-2	1,251	–	18 MHz	Available Now
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

V6502 Microprocessor

VAutomation
See profile on page 70.

Applications

- Buses & Interfaces
- ✓ Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- Code-compatible with the Rockwell R65C02
- 70 instructions, 210 opcodes, 15 addressing modes
- 8-bit ALU with binary and decimal arithmetic
- 64-Kbyte addressing capability
- Fully synchronous and static design

The V6502 microprocessor megafunction is a high-performance, 8-bit microprocessor. The megafunction is functionally based on—and compatible with—the Rockwell R65C02. In addition, assemblers and C compilers are available for the megafunction from third-party developers.

The V6502 microprocessor megafunction has been completely redesigned using the latest high-speed design techniques to produce a high-performance microprocessor with a minimal gate count. The megafunction is easily integrated with user-specified logic and other megafunctions.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K						Consult Partner
FLEX 8000						Consult Partner
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

C68450 DMA Controller

CAST
See profile on page 62.

Applications

- Buses & Interfaces
- ✓ Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- Four independent DMA channels
- Programmable channel prioritization
- Array-chained and linked-chained operations
- Auto-request and external-request transfer modes
- Two-vectored interrupts for each channel

The C68450 DMA Controller megafunction complements the performance and architecture of the M68000 family of microprocessors. The megafunction is designed to move blocks of data in a quick and efficient manner. The megafunction supports four independent DMA channels, and implements memory-to-memory, memory-to-device, and device-to-memory data transfers.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K						Q1 1997
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

C6850 Asynchronous Communications Interface Adapter

CAST
See profile on page 62.

Applications

- Buses & Interfaces
- ✓ Processor & Peripherals
- ✓ Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- Programmable data word length, parity, and stop bits
- Parity, overrun, and framing error checking
- Transmission rates greater than an order of magnitude are faster than standard product 6850
- False start-bit deletion
- Peripheral modem control functions

The C6850 asynchronous communications interface adapter (ACIA) megafunction provides data formatting and control to the asynchronous data communications of data bus systems.

The megafunction has select, enable, read/write, interrupt, and bus interface logic features that allow data transfers over an 8-bit bidirectional parallel data bus system. With proper formatting and error checking, the megafunction can transmit and receive serial data.

A programmable control register provides a transmit control, a receive control, an interrupt control, variable word lengths, and clock division ratios. Three control lines are provided for peripheral or modem operation.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K	EPF10K10	-3	188	0	34.48 MHz	Q1 1997
FLEX 8000	EPF8282A	A-2	188	–	33.78 MHz	Q1 1997
MAX 9000	EPM7160E	-10	135	–	22.72 MHz	Q1 1997
MAX 7000	EPM9320	-15	153	–	21.45 MHz	Q1 1997

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

VZ80 Microprocessor

VAutomation
See profile on page 70.

Applications

- Buses & Interfaces
- ✓ Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- Code-compatible with Zilog Z80
- 158 instructions, 10 addressing modes
- 8-bit ALU with binary and decimal arithmetic
- 64-Kbyte addressing capability
- Fully synchronous and static design

The VZ80 microprocessor megafunction is a powerful, medium-gate-count microprocessor that includes block transfers, and bit test, set, and reset instructions. The megafunction is functionally based on—and compatible with—the Zilog Z80. In addition, assemblers and C compilers are available for the megafunction from third-party developers.

The megafunction has fast context switch capability with an entire auxiliary register set. The megafunction is easily integrated with user-specified logic and other megafunctions.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K						Consult Partner
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

C8051 Microcontroller

CAST

See profile on page 62.

Applications

- Buses & Interfaces
- ✓ Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- 128 × 8-bit RAM
- 64 K memory addressing capability
- Two 16-bit counter/timers
- Full duplex serial channel

The C8051 microcontroller megafunction implements a standard 8051 microcontroller. The megafunction supports the following standard features: 8051 architecture instruction set, 128 × 8-bit RAM, 32 I/O lines, two 16-bit counter/timers, and a five-source/two priority-level nested interrupt structure.

The megafunction has a serial I/O port for multi-processor communications (I/O expansion or full duplex UART).

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K						Q1 1997
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

RAW8051-A

Richard Watts Associates
See profile on page 79.

Applications

- Buses & Interfaces
- ✓ Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- Fast 8051/31 megafunction with 100% software code compatibility
- Includes standard 8051 peripherals
- Three times faster than a standard product 8051
- Reduced execution cycle time
- ASIC versions available for easy migration
- Evaluation board available for prototyping

The RAW8051-A megafunction implements an enhanced industry-standard, 8051 8-bit microcontroller. On average, the megafunction executes software three times faster than a standard 8051 while maintaining 100% software code compatibility.

The megafunction includes the following standard 8051 peripherals: 1 full-duplex serial UART, 2 16-bit timer/counters, 32 I/O lines, idle and power down modes, and a 6-source/5-vector nested interrupt structure with two priority levels. A Philips-compatible extra data pointer is provided for faster memory copies and indexing.

The RAW8051-A megafunction is supported by a wide variety of standard EDA development tools. The megafunction allows designers to use existing software code and achieve performance that is comparable to RISC megafunctions.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K40	-3	1,825	1	9.42 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example is optimized for minimum area. Speed improvements are possible.

RAW8052-A

Richard Watts Associates
See profile on page 79.

Applications

- Buses & Interfaces
- ✓ Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- Fast 8052/32 megafunction with 100% software code compatibility
- Includes standard 8052 peripherals
- Three times faster than a standard product 8052
- Reduced execution cycle time
- ASIC versions available for easy migration
- Evaluation board available for prototyping

The RAW8052-A megafunction implements an enhanced industry-standard, 8052 8-bit microcontroller. On average, the megafunction executes software three times faster than a standard 8052 while maintaining 100% software code compatibility.

The megafunction includes the following standard 8052 peripherals: 1 full-duplex serial UART, 3 16-bit timer/counters, 32 I/O lines, idle and power down modes, and a 7-source/6-vector nested interrupt structure with two priority levels. A Philips-compatible extra data pointer is provided for faster memory copies and indexing.

The RAW8052-A megafunction is supported by a wide variety of standard EDA development tools. The megafunction allows designers to use existing software code and achieve performance that is comparable to RISC megafunctions.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K40	-3	2,000	1	8.45 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example is optimized for minimum area. Speed improvements are possible.

BareCore 8052-A

Richard Watts Associates
See profile on page 79.

Applications

- Buses & Interfaces
- ✓ Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- Fast 8052/32 CPU-only with 100% software code compatibility
- Three times faster than a standard product 8052
- Reduced execution cycle time
- ASIC versions available for easy migration
- Evaluation board available for prototyping

The BareCore 8052-A megafunction implements an enhanced industry-standard, 8052 8-bit microcontroller. On average, the megafunction executes software three times faster than a standard 8052 while maintaining 100% software code compatibility. A Philips-compatible extra data pointer is provided for faster memory copies and indexing.

The BareCore 8052-A megafunction is supported by a wide variety of standard EDA development tools.The megafunction allows designers to use existing software code and achieve performance that is comparable to RISC megafunctions.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K30	-3	1,400	1	10.58 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example is optimized for minimum area. Speed improvements are possible.

C8255A Programmable Peripheral Interface

CAST
See profile on page 62.

Applications

- Buses & Interfaces
- ✓ Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- 8255-compatible programmable peripheral interface (PPI)
- 24 programmable I/O pins
- Direct bit set/reset capability
- Three basic modes of operation
- Functionally based on the Intel 8255A device

The C8255A programmable peripheral interface megafunction implements a general-purpose I/O interface to connect peripheral equipment to a microcomputer system bus. The megafunction's functional configuration is programmed by the system software so that external logic is not required to interface peripheral devices.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K						Q1 1997
FLEX 8000						Q1 1997
MAX 9000						Q1 1997
MAX 7000						Q1 1997

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

Adaptive Filters

Integrated Silicon Systems
See profile on page 70.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- ✓ DSP for Imaging
- ✓ DSP for Communications

- Sample rates ranging from 2 kHz to over 75 MHz
- Fully parameterized adaptive filters
- Both 1-D and 2-D variants available
- Optimized to provide desired functionality with minimum silicon
- "On-the-fly" coefficient adaptation available
- Applications include:
  - 1-D and 2-D adaptive filtering
  - Image and video processing
  - Pulse shaping
  - Correlation and equalization

The adaptive filter megafunctions, with sample rates ranging from 2 kHz to over 75 MHz, are ideal for solving filtering problems.

The megafunctions are optimized for implementation in FLEX 10K devices, and can be customized to meet user specifications. ISS can customize the number of filter taps, filter dimensions (e.g., 1-D or 2-D), performance (pipelining), data word lengths and formats, filter structure, and adaptation rule (including custom rules and the LMS algorithm).

ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K50	-3	2,010	0	60 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example has 8 taps, 8-bit input data, 8-bit coefficients, 20-bit output, LMS algorithm, and a sample rate of 60 MSPS.

Binary Pattern Correlator

Nova Engineering
See profile on page 75.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- ✓ DSP for Communications

- Detects a reference pattern within a data stream
- Programmable threshold register
- Parameterized reference pattern length and width
- Pipelined architecture for maximum speed
- Applications include:
  - Spread spectrum communications
  - Pattern recognition
  - Error correction
  - Frame synchronization

The binary pattern correlator megafunction is designed to search a serial data stream for the presence of a user-programmed reference pattern. The reference pattern is detected when the number of matches between the reference pattern and the input data exceeds the threshold value. Threshold values allow the user to program the acceptable tolerance for a pattern match.

The binary pattern correlator megafunction uses a parallel and pipelined architecture that provides maximum speed. The megafunction's internal and external operations are synchronized to the rising clock edge, and an asynchronous reset input is provided for initializing all internal registers.

Nova Engineering will customize the megafunction's reference pattern length and width at no additional cost. Customizing the data widths will optimize the megafunction for specific applications.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K						Q2 1997
FLEX 8000						Q2 1997
MAX 9000						Q2 1997
MAX 7000	–	–	–	–	–	–

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

Biorthogonal Wavelet Filter

FASTMAN
See profile on page 69.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- ✓ DSP for Imaging
- DSP for Communications

- Low-pass/high-pass filter integration
- Pipelined design
- Parallel vector multipliers
- Very fast implementation
- Biorthogonal symmetric filters
- Applications include:
  - Fingerprint compression
  - Advanced image compression

The biorthogonal wavelet filter megafunction operates on an incoming data stream and produces an output stream that consists of alternating low-pass and high-pass filtered outputs, each decimated by a factor of two from the input.

The megafunction has a simple interface consisting of data input and output registers and a single global clock, and it employs fast pipelined parallel vector multipliers. The internal clock runs at one half of the input data clock speed.

The biorthogonal wavelet filter megafunction is symmetrical, which makes it ideal for image processing applications. Other types of wavelet filter megafunctions are available through FASTMAN's custom design program.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K40	-4	1,776	0	68 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example has a 16-bit data size and 12-bit coefficient precision.

C_UART

CAST
See profile on page 62.

Applications

- Buses & Interfaces
- ✓ Processor & Peripherals
- ✓ Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- 8-bit characters
- T × C/R × C (16 times the desired output baud rate)
- 1 start bit/1 stop bit
- Polling and interrupt modes
- Flexibility for adding other features

The C_UART megafunction is a generic universal asynchronous receiver/transmitter (UART) and can be used to implement a peripheral data communications device. The designer can program the megafunction with an 8-bit CPU.

Features such as character length, parity, and programmable start/stop bits can be easily added into the megafunction. Contact CAST for customization information.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K	EPF10K10	-3	104	0	71.94 MHz	Available Now
FLEX 8000	EPF8282A	A-2	91	–	61.72 MHz	Available Now
MAX 9000	EPM7160E	-10	58	–	62.50 MHz	Available Now
MAX 7000	EPM9320	-15	58	–	43.10 MHz	Available Now

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

Complex Multiplier/Mixer

Nova Engineering
See profile on page 75.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- ✓ DSP for Communications

- Multiplies/mixes two complex numbers/signals
- Fully synchronous design
- Parameterized data width
- Parallel implementation for maximum speed
- Applications include:
  - Digital mixers
  - Modulators/demodulators
  - Discrete Fourier transforms (DFTs)
  - Complex arithmetic
  - Wireless communications systems

The complex multiplier/mixer megafunction multiplies two complex numbers or mixes two complex signals. It has a parallel, pipelined architecture that maximizes speed. The megafunction's internal and external operations are synchronized to the rising clock edge, and an asynchronous reset input is provided for initializing all internal registers.

The megafunction can be used for vector cross products, vector dot products, up/down frequency conversion, differential phase detection, digital amplitude modulation (AM), quadrature amplitude modulation (QAM), and DFT. The megafunction does not require FLEX 10K EABs, and therefore, it can be combined with sine/cosine look-up tables (LUTs) for frequency down conversion or DFT functions within a single device.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K20	-3	604	0	60 MHz	Available Now
FLEX 8000, *Note (2)*	EPF81188A	A-2	604	–	55 MHz	Available Now
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example has an 8 × 8 complex multiplier with 3 clock latency.

Convolution Interleaver

KTech Telecommunications
See profile on page 72.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- ✓ DSP for Communications

- Convolutional interleaver function
- Bit byte is accepted at each clock cycle
- Interleaved 8-bit byte produced at each clock cycle
- Applications include:
  - Personal communications systems (PCS)
  - Cable modems

The convolution interleaver megafunction implements a convolutional interleaver that is optimized for PCS and cable modem applications. For small interleaving depth, the megafunction uses FLEX 10K EABs. For large interleaving depth, the megafunction requires an external dual-port RAM and ROM.

The megafunction accepts the input signal 8 bits at a time. At each byte clock cycle, the input and output selector arms shift to the next set of data. When the final index *N* is reached, the selector arms go back to the initial index 1 arm, and the selector arms continue with each byte cycle. After the latency introduced by the interleaver, the output produces 8 bits at a time.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K	EPF10K10	-4	252	0	52 MHz	Available Now
FLEX 8000	EPF8452A	A-2	244	–	66 MHz	Available Now
MAX 9000	EPM9320	-12	185	–	85 MHz	Available Now
MAX 7000						Consult Partner

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

Decimating Filter

FASTMAN
See profile on page 69.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- ✓ DSP for Imaging
- ✓ DSP for Communications

- Uses parallel vector multipliers
- Pipelined design
- Symmetrical or asymmetrical
- Even or odd number of taps
- Fast parallel implementation
- Customizable number of taps, data word size, and internal precision
- Applications include:
  - MPEG audio
  - Band-pass filtering

The decimating filter megafunction implements biorthogonal wavelet filters for signal processing or compression. The megafunction operates on an incoming data stream, and it produces a filtered output stream that is decimated by a factor of two.

The designer can select the number of taps, the data word size, and the internal precision for the megafunction. In addition, the designer can select any set of filter coefficients and input them into the design through a data file. The megafunction can implement a filter with an even or odd number of taps in a symmetrical or asymmetrical manner. When the number of taps is odd, the filter is symmetrical to the center tap. The filter employs pipelined parallel vector multipliers. The internal clock of the filter runs at the output clock speed (i.e., one half of the input clock speed).

FASTMAN can customize a wide variety of filters (including non-decimating filters) to meet user specifications.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K20	-3	1,040	0	65.0 MHz	Available Now
FLEX 10K, *Note (3)*	EPF10K20	-3	921	0	62.5 MHz	Available Now
FLEX 8000, *Note (4)*	EPF8820A	A-2	185	–	77.5 MHz	Available Now
FLEX 8000, *Note (5)*	EPF81500A	A-2	920	–	55.0 MHz	Available Now

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example has a 9-tap filter and 16-bit data word size.
(3) This example has a 5-tap filter and 16-bit data word size.
(4) This example has a 8-tap filter and 8-bit data word size.
(5) This example has a 5-tap filter and 16-bit data word size.

Digital Modulator

Nova Engineering
See profile on page 75.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- ✓ DSP for Communications

- Implements a wide variety of modulation formats
- Uses phase-continuous direct digital synthesis (DDS)
- Parameterized input and output data widths for specific applications
- Optimized for the FLEX 10K device architecture
- Applications include:
  - Amplitude modulators
  - Frequency modulators
  - Phase modulators
  - Up/down frequency conversion

The digital modulator megafunction combines a quadrature numerically controlled oscillator (NCO) with a complex multiplier/mixer to provide a wide tuning range and excellent frequency resolution, and a fast settling time. The megafunction's parallel and pipelined architecture maximizes speed.

The megafunction generates a wide variety of modulation formats, including: amplitude modulation (AM), frequency modulation (FM), amplitude shift keying (ASK), frequency shift keying (FSK), continuous phase modulation (CPM), and phase shift keying (PSK).

Nova Engineering will customize the phase accumulator width, multiplier width, phase offset input width, and the output data width at no additional charge.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K20	-3	666	2	54 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example has a 24-bit accumulator, 10-bit phase offset, 8-bit complex multiplier, and 8-bit quadrature outputs.

Discrete Cosine Transform

Integrated Silicon Systems
See profile on page 70.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- ✓ DSP for Imaging
- DSP for Communications

- Fully parameterized megafunction
- DCT, IDCT, and combined DCT/IDCT variants available
- High performance (up to 50 MHz)
- Implements an 8 × 8 2-D DCT conforming to many image compression standards
- Applications include:
  - Multimedia systems
  - Set-top boxes,
  - Video telephony systems
  - Broadcast systems

The discrete cosine transform (DCT) megafunctions can operate at sample rates of up to 50 MHz, and are fundamental building blocks for many image and video compression systems. Additional functionality ensures that the megafunctions are easy to use and reduces the requirement for extra circuitry in systems development. Parameter selection enables the megafunctions to comply with the following standards: H.261, H.263, JPEG, MPEG-1, MPEG-2, and MPEG-4.

ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K100	-3	4,386	0	17.45 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example is an 8 × 8 2-D DCT with 8-bit input, 8-bit output, 8-bit coefficient word lengths, and 12-bit internal precision.

Early/Late-Gate Symbol Synchronizer

Nova Engineering
See profile on page 75.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- ✓ DSP for Communications

- Aligns local clock phase to incoming binary data transitions
- Supports a wide range of sample clock rates
- Includes programmable loop filter
- Supports acquisition and tracking modes
- Applications include:
  - Digital receivers
  - Synchronous data interfaces

The early/late-gate symbol synchronizer megafunction is a closed loop binary data synchronizer that performs two separate integrations for each symbol interval. The integrators accumulate the value of the symbol—detected at the sample clock rising edge—for each half of the symbol period. The difference between the integration is a measure of the local clock timing error. When the first half symbol integration matches the second half symbol integration, the local data clock is aligned to the incoming data.

The megafunction includes a filter for controlling the timing loop response. The filter can be programmed to increase the loop bandwidth, which provides a faster transient response during acquisition mode. The loop bandwidth can also be reduced to provide better performance during tracking mode.

A programmable clock divider allows the megafunction to support a wide range of sample clock rates. Increasing the sample clock rate provides finer timing resolution and subsequently, less timing jitter. Decreasing the sample clock rate reduces power consumption, particularly in applications where timing jitter requirements are less stringent.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K						Q2 1997
FLEX 8000						Q2 1997
MAX 9000						Q2 1997
MAX 7000	–	–	–	–	–	–

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

FIR Filter Library

Integrated Silicon Systems
See profile on page 70.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- ✓ DSP for Imaging
- ✓ DSP for Communications

- Sample rates ranging from 2 kHz to over 75 MHz
- Fully parameterized finite impulse response (FIR) filters
- Both 1-D and 2-D variants available
- Optimized to provide desired functionality with minimum silicon
- "On-the-fly" coefficient adaptation available
- Applications include:
  - 1-D and 2-D FIR filtering
  - Matched filtering
  - Adaptive filtering
  - Image and video processing
  - Pulse shaping
  - Correlation and equalization

The megafunctions in the FIR filter library, with sample rates ranging from 2 kHz to over 75 MHz, are ideal for solving filtering problems. By cascading the megafunctions, the designer can construct large high-speed FIR filters. The megafunctions can also be replicated to construct a range of FIR filters, which are all covered by the same FIR filter library license.

ISS can customize the number of filter taps, filter dimensions (e.g., 1-D or 2-D), performance (pipelining), and data word lengths and formats. ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K40	-3	1,827	0	60.6 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example has an 8-bit input data, 8-bit coefficients, full internal accuracy, "on-the-fly" coefficient adaptation, and is cascadable to create larger filters.

Floating-Point Adder

Integrated Silicon Systems
See profile on page 70.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- ✓ DSP for Imaging
- ✓ DSP for Communications

- Fully parameterized exponent, mantissa, and pipeline architecture
- High performance
- Small size
- Applications include:
  - Adaptive systems
  - Safety-critical systems
  - Flight control, guidance, and scientific processing

The floating-point adder megafunction is used in all data processing areas that require accurate calculation beyond what can be achieved with fixed-point processing.

ISS can customize the megafunction to meet specific application requirements. ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K20	-3	616	0	19.92 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example has a 16-bit mantissa, 6-bit exponent, and 3 levels of pipelining.

Floating-Point Divider

Integrated Silicon Systems
See profile on page 70.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- ✓ DSP for Imaging
- ✓ DSP for Communications

- Fully parameterized exponent, mantissa, and pipeline architecture
- High performance
- Small size
- Applications include:
  - Adaptive systems
  - Safety-critical systems
  - Flight control, guidance, and scientific processing

The floating-point divider megafunction is used in all data processing areas that require accurate calculation beyond what can be achieved with fixed-point processing.

ISS can customize the megafunction to meet specific application requirements. ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K40	-3	1,930	0	22.12 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example has a 16-bit mantissa, 6-bit exponent, and 12 levels of pipelining (maximum 20 levels).

Floating-Point Multiplier

Integrated Silicon Systems
See profile on page 70.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- ✓ DSP for Imaging
- ✓ DSP for Communications

- Fully parameterized exponent, mantissa, and pipeline architecture
- High performance
- Small size
- Applications include:
  - Adaptive systems
  - Safety-critical systems
  - Flight control, guidance, and scientific processing

The floating-point multiplier megafunction is used in all data processing areas that require accurate calculation beyond what can be achieved with fixed-point processing.

ISS can customize the megafunction to meet specific application requirements. ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K10	-3	226	0	29.41 MHz	Available Now
FLEX 10K, *Note (3)*	EPF10K20	-3	849	0	21.23 MHz	Available Now
FLEX 8000, *Note (2)*	EPF8452A	A-3	223	–	24.44 MHz	Available Now
FLEX 8000, *Note (3)*	EPF8118A	A-2	866	–	17.92 MHz	Available Now

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example has an 8-bit mantissa, 6-bit exponent, and 2 levels of pipelining (maximum 3 levels).
(3) This example has a 16-bit mantissa, 6-bit exponent, and 2 levels of pipelining (maximum 3 levels).

HDLC Controller

Integrated Silicon Systems
See profile on page 70.

Applications

- Buses & Interfaces
- Processor & Peripherals
- ✓ Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- Formats data to various standards (e.g., X.25 CCITT level-2)
- Uses handshake signals for multiplexing data links
- High-speed serial output
- Includes microprocessor interface
- Applications include:
  - Digital sets, PBX, and private packet networks
  - C-channel controller to Digital Network Interface Circuits
  - D-channel controller for ISDN basic access
  - Inter-processor communication
  - Data link controllers and protocol generators

The HDLC controller megafunction transmits and receives packeted data for communication. The megafunction features include: go-ahead sequence generation and detection, function protocol disable operation, single-byte address recognition, watchdog timer, and twin FIFOs for send and receive paths.

The megafunction can be delivered in several configurations to meet specific communication standard requirements. ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K						Q2 1997
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

IIR Filter Library

Integrated Silicon Systems
See profile on page 70.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- ✓ DSP for Imaging
- ✓ DSP for Communications

- Fully parameterized
- Cascadable
- High performance
- "On-the-fly" coefficient adaptation available
- Applications include:
  - Digital audio processing
  - Digital video processing
  - Signal conditioning
  - Channel selection filtering

The megafunctions in the IIR filter library are used in a broad spectrum of signal bandwidths. The megafunctions are basic building blocks for many IIR filter implementations. A second-order IIR filter—such as a biquad—can be used to construct higher orders of filter by cascading the required number of biquad sections. A complete range of high performance IIR filters can be constructed from a single IIR filter megafunction, which is covered under the same IIR filter library license.

ISS can customize the data sample rate, coefficient loading strategy, filter order, and data word lengths and formats. The megafunctions can process data at rates in excess of 50 MSPS. Contact ISS for the best parameter settings to meet specific application requirements.

ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K20	-5	430	6	17 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example is a biquad IIR filter with an 8-bit input, 8-bit coefficients, and11-bit internal accuracy.

Image Processing Library

Integrated Silicon Systems
See profile on page 70.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- ✓ DSP for Imaging
- DSP for Communications

- Wide range of front-end video and image processing megafunctions
- Parameterized level of pipelining, window sizes, and data word lengths and formats
- Option to use FLEX 10K EABs as pixel line delays
- Real-time operation with pixel rates up to and including HDTV standard rate of 54 MHz

The image processing library includes the following front-end video and image processing megafunctions: edge detectors, image enhancement filters, matched filters, video convolvers, contrast enhancement filters, and median filters. These image processing megafunctions have been simplified to reduce the interface requirements and to enable the rapid generation of high quality, high functionality, real-time processing designs.

An image processing megafunction can use FLEX 10K EABs to implement the required line delays for 2-D filtering applications. Also, several front-end image processing megafunctions can be incorporated in a single design, allowing developers to perform multiple processing tasks in real-time and to switch instantaneously between them. Contact ISS for the best parameter settings to meet specific application requirements.

ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K10	-3	231	0	90.0 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:

(1) Specifications are subject to change. See page 11 for more information regarding this table.

(2) This example is a 3 × 3 Laplacian edge detector with an 8-bit unsigned binary data input and 12-bit signed binary output. It operates on a sliding window, producing a result for each pixel.

Integer Divider

Integrated Silicon Systems
See profile on page 70.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- ✓ DSP for Imaging
- ✓ DSP for Communications

- Fully parameterized megafunction
- Overflow detection
- High performance
- Small size
- Applications include:
  - Digital signal processing
  - Control processing
  - Data processing

When used with other mathematical operators, the integer divider megafunction enables complex systems and calculations to be implemented in programmable logic. The megafunction accelerates calculation operations by orders of magnitude. The megafunction also has an overflow detection feature.

ISS can customize the performance, data word length, and format requirements for specific applications. ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K20	-3	801	0	38.16 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example has a 12-bit dividend, 12-bit divisor, 13-bit quotient, and pipelining = 9 (maximum pipelining = 17).

JPEG Decoder & Encoder

Integrated Silicon Systems
See profile on page 70.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- ✓ DSP for Imaging
- DSP for Communications

- Parameterized megafunction to match system requirements
- Highly flexible system-level components
- High performance
- Applications include:
  - Digital camera technology
  - Digital image archiving
  - Document imaging
  - Multimedia applications
  - Still image transmission

The JPEG decoder and encoder megafunctions can be implemented into FLEX 10K device architectures. The megafunctions can be parameterized to match any system that requires high performance and flexible JPEG decoding and encoding.

ISS can customize the decoding and encoding rates and the data word lengths to meet specific application requirements. ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K						Q2 1997
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

JPEG Decoder & Encoder

Synova
See profile on page 69.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- ✓ DSP for Imaging
- DSP for Communications

- High-speed JPEG decoder and encoder
- On-chip buffer RAM
- Programmable tables
- Programmable inverse DCT coefficients
- 8-bit input data width

The JPEG decoder and encoder megafunctions provide a high-speed hardware implementation of the JPEG baseline image decompression algorithm. These megafunctions are targeted for real-time imaging applications.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K						Q1 1997
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

Linear Feedback Shift Register

Nova Engineering
See profile on page 75.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- ✓ DSP for Communications

- Programmable register length and initial value
- Automatic resizing and feedback selection (2 to 32 bits)
- Feedback architecture designed for maximum speed
- Multiple user-selectable configurations
- Applications include:
  - Direct sequence spread spectrum (DSSS)
  - Pseudo-random number (PN) generation
  - Built-in self test (BIST)
  - Encryption/decryption
  - Error detection

The linear feedback shift register (LFSR) megafunction is based on linear XOR or XNOR feedback logic in which the initial value of the shift register, shift register taps, and feedback logic determines the output sequence. The megafunction can be resized to any length between 2 and 32 bits, and the feedback logic automatically adapts to the shift register length to produce a maximal length sequence.

The LFSR megafunction is designed to provide feedback delays that are independently reconfigured. This architecture maximizes speed and provides uniform performance for all configurations.

Nova Engineering will customize the LFSR megafunction's shift register size and the feedback configuration to meet user specifications at no additional cost. This customization reduces logic usage and optimizes area and performance.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K	EPF10K10	-4	317	0	86 MHz	Available Now
FLEX 8000	EPF8452A	A-3	309	–	50 MHz	Available Now
MAX 9000	EPM9320	-15	103	–	74 MHz	Available Now
MAX 7000	EPM7128E	-10	103	–	92 MHz	Available Now

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

Median Filter Library

Integrated Silicon Systems
See profile on page 70.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- ✓ DSP for Imaging
- ✓ DSP for Communications

- Fixed and programmable median filter
- Highly parameterizable
- Both 1-D and 2-D variant options available
- High performance

The median filter library includes 1-D and 2-D variants that support a wide range of applications. The megafunctions are typically used in audio and video applications, where this form of data reorganization can improve the quality of the signals.

ISS can customize that megafunction to meet specific application requirements. Programmable median filters (an additional option) can handle both 1-D and 2-D data. ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K20	-3	588	0	25 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example is a 3 × 3 filter with an 8-bit input.

Multi-Standard ADPCM

Integrated Silicon Systems
See profile on page 70.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- ✓ DSP for Communications

- Compliant with G.721, G.723, G.726, G.726a, G.727, and G.727a ITU standards
- Coding 64 kbits/second to and from 40, 32, 24, and 16 kbits/second
- Support for both A-and µ-law PCM coding
- Support for up to 20 full duplex channels, and 40 encode or decode channels
- Applications include:
  - Overload voice channels in digital circuit multiplication equipment (DCME)
  - Data modems for DCME
  - Packetized voice protocol (PVP) systems.

The multi-standard adaptive pulse code modulation (ADPCM) megafunction performs multi-channel duplex ADPCM coding in telecommunications applications. If the designer requires only a subset of the megafunction's capabilities, the Altera MAX+PLUS II software program will remove unused logic during logic synthesis. This feature improves device utilization and facilitates system development and prototyping on a FLEX 10K device.

The megafunction's functionality and timing are verified using ITU standard test sequences. ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K100	-3	3,963	5	5.12 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example has 16 channels, and full duplex coding that has all standards and coding rates and supports PCM laws.

Numerically Controlled Oscillator

Nova Engineering
See profile on page 75.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- ✓ DSP for Communications

- Optimized for FLEX 10K embedded array blocks (EABs)
- Generates digital sine and cosine waveforms
- Simultaneous quadrature outputs
- Parameterized phase accumulator width and output data width
- Applications include:
  - Direct digital synthesis (DDS) for up/down frequency conversion
  - Frequency hopping systems
  - Discrete Fourier transforms (DFTs)
  - Polar to rectangular conversion
  - Digital modulation/demodulation

The numerically controlled oscillator (NCO) megafunction generates digital sine and cosine waveforms at a programmable periodic rate. The sine and cosine outputs can be adjusted over a wide range of frequencies, with a high degree of resolution. The megafunction's frequency resolution and tuning range are determined by the phase accumulator width and system clock. The megafunction's simultaneous quadrature outputs are ideal for quadrature modulation formats such as quadrature phase shift keying (QPSK) and quadrature amplitude modulation (QAM).

Nova Engineering will customize the phase accumulator and output data widths to user specifications at no additional charge. Customizing the phase accumulator width and output data width optimizes the megafunction for specific applications.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K10	-3	60	2	58 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example has a phase accumulator width of 24 bits and an output data width of 8 bits for sine and cosine outputs.

PCI Bus Master (EC200)

Eureka Technology
See profile on page 65.

Applications

- ✓ Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- Fully compliant with PCI-SIG 2.1 ***PCI Local Bus Specification***
- Supports burst mode data transfer
- Provides bus target capability for device setup
- 33-MHz operating frequency

The PCI bus master megafunction(EC200) provides an interface between a bus mastering device and a PCI bus. The megafunction translates all data requests from the coprocessor to the PCI interface. All PCI configuration registers are included in the megafunction, and configuration requests are processed locally by the megafunction.

The megafunction also provides PCI target capability for the control register setup of a bus mastering device (i.e., DMA controller or video coprocessor).

The megafunction is available in AHDL, Verilog HDL, and VHDL. Eureka Technology can customize the megafunction to meet specific user requirements. Contact Eureka Technology for a complete data sheet.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K	EPF10K10	-3	*Note (2)*	0	33 MHz	Available Now
FLEX 8000	EPF8820A	A-2	*Note (2)*	–	33 MHz	Available Now
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) Megafunction sizes vary with feature addition/deletion and customization. Contact the partner for an LC count that is based on user specifications.

32-Bit PCI Bus Master/Target

Logic Innovations
See profile on page 73.

Applications

- ✓ Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- Optimized for FLEX 10K device architectures
- Master interface, plus memory mapped bus target
- Fully compliant PCI configuration space
- Burst memory transfer as master
- PCI/local SRAM-based memory queue implemented in EABs

The 32-bit PCI Bus master/target megafunction provides resident core memory-mapped DMA control, address counter, byte-count register, interrupt status register, and configurable PCI interrupt source generation (i.e., transfer complete, local side, parity error, and master/target abort). A simple back-end interface controls DMA requests.

The megafunction is available as a VHDL-based source code package, which includes detailed documentation and a complete PCI test bench. An optional evaluation board with schematics is also available. Logic Innovations can customize the megafunction to meet specific user requirements.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K	EPF10K20	-3	850	4	33 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

PCI Bus Target (EC100)

Eureka Technology
See profile on page 65.

Applications

- ✓ Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- Fully compliant with PCI-SIG 2.1 ***PCI Local Bus Specification***
- Supports burst mode data transfer
- Internal write buffer to maximize data bandwidth
- Optional FIFO interface
- 33-MHz operating frequency

The PCI Bus Target megafunction (EC100) provides an interface between a target device and a PCI bus. The megafunction performs all data transfer functions requested by the PCI bus master. To maximize data bandwidth, the megafunction provides an internal write buffer and supports burst mode data transfer. All PCI configuration registers are included in the megafunction, and configuration requests are processed locally by the megafunction.

The megafunction is available in AHDL, Verilog HDL, and VHDL. Eureka Technology can customize the megafunction to meet user specifications. Contact Eureka Technology for a complete data sheet.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K	EPF10K10	-3	*Note (2)*	0	33 MHz	Available Now
FLEX 8000	EPF8636A	A-2	*Note (2)*	–	33 MHz	Available Now
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) Megafunction sizes vary with feature addition/deletion and customization. Contact the partner for an LC count that is based on user specifications.

PowerPC Bus Arbiter (EP300)

Eureka Technology
See profile on page 65.

Applications

- ✓ Buses & Interfaces
- ✓ Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- Compatible with any 60*x*-compliant bus architecture
- Manages up to 8 bus masters
- Supports address pipelining and retry
- Fixed and rotating priority

The PowerPC bus arbiter megafunction (EP300) arbitrates the PowerPC address and data buses to allow multiple bus masters or processors to co-exist on the host bus. The megafunction is designed for the PowerPC host bus and works with any 60*x*-compliant bus architecture. The megafunction can be used as a stand-alone function or it can be incorporated in the same device with the bus master or slaves. Both fixed and round-robin priority schemes can be implemented with the arbiter.

To improve system performance, the megafunction supports advanced features of the PowerPC bus such as address pipelining, address retry, bus parking, and separate arbitration for the address and data buses. The megafunction allows address pipelining with two outstanding memory accesses.

The megafunction is available in AHDL, Verilog HDL, and VHDL. Eureka can customize the megafunction to meet user specifications. Contact Eureka for a complete data sheet.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K	EPF10K10	-3	*Note (2)*	0	50 MHz	Available Now
FLEX 8000	EPF8282A	A-2	*Note (2)*	–	50 MHz	Available Now
MAX 9000						Consult Partner
MAX 7000						Consult Partner

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) Megafunction sizes vary with feature addition/deletion and customization. Contact partner for an LC count that is based on user specifications.

PowerPC Bus Master (EP200)

Eureka Technology
See profile on page 65.

Applications

- ✓ Buses & Interfaces
- ✓ Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- Compatible with any 60*x*-compliant bus architecture
- Handles all PowerPC bus protocols
- Supports address pipelining and retry

The PowerPC bus master megafunction (EP200) is an external master that resides directly on the PowerPC host bus. The megafunction is designed for the PowerPC host bus and works with any 60*x*-compliant bus architecture. A simple and efficient back bus provides an interface to the user logic that initiates bus access. The megafunction can simultaneously handle all the PowerPC bus protocols.

To improve system performance, the megafunction supports advanced features of the PowerPC bus such as address pipelining, address retry, bus parking, and separate arbitration for the address and data buses. The megafunction also supports both single beat and burst data transfers, and it allows address pipelining with two outstanding memory accesses.

The megafunction is available in AHDL, Verilog HDL, and VHDL. Eureka can customize the megafunction to meet user specifications. Contact Eureka for a complete data sheet.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K	EPF10K10	-3	*Note (2)*	0	50 MHz	Available Now
FLEX 8000	EPF8282A	A-2	*Note (2)*	–	50 MHz	Available Now
MAX 9000						Consult Partner
MAX 7000						Consult Partner

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) Megafunction sizes vary with feature addition/deletion and customization. Contact partner for an LC count that is based on user specifications.

PowerPC Bus Slave (EP100)

Eureka Technology
See profile on page 65.

Applications

- ✓ Buses & Interfaces
- ✓ Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- Compatible with any 60*x*-compliant bus architecture
- Supports data bursting with standard asynchronous SRAM
- Supports address pipelining and retry

The PowerPC bus slave megafunction (EP100) provides a slave memory controller and supports standard asynchronous SRAM devices. The megafunction is designed for the PowerPC host bus and works with any 60*x*-compliant bus architecture. The megafunction allows a memory subsystem built with standard SRAM to be connected to the PowerPC host bus. To achieve the highest possible bandwidth, the megafunction also emulates data bursting capability.

To improve system performance, the megafunction supports advanced features of the PowerPC bus such as address pipelining, address retry, bus parking, and separate arbitration for the address and data buses. The megafunction also supports both single beat and burst data transfer, and it allows address pipelining with two outstanding memory accesses.

The megafunction is available in AHDL, Verilog HDL, and VHDL. Eureka can customize the megafunction to meet user specifications. Contact Eureka for a complete data sheet.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K	EPF10K10	-3	*Note (2)*	0	50 MHz	Available Now
FLEX 8000	EPF8282A	A-2	*Note (2)*	–	50 MHz	Available Now
MAX 9000						Consult Partner
MAX 7000						Consult Partner

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) Megafunction sizes vary with feature addition/deletion and customization. Contact the partner for an LC count that is based on user specifications.

Rank Order Filter Library

Integrated Silicon Systems
See profile on page 70.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- ✓ DSP for Imaging
- ✓ DSP for Communications

- Fixed and programmable rank order filter megafunctions
- Highly parameterizable
- Both 1-D and 2-D variants available
- High performance

The rank order filter library includes 1-D and 2-D variants, which support a wide range of applications. The programmable rank order filters can handle 1-D and 2-D data. The megafunctions are typically used in audio and video applications, where this form of data re-organization can improve the quality of the signals.

The rank order filters can be parameterized to match specific system requirements. ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K100	-3	3,852	0	25 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example is a programmable filter with a window of up to 15 × 1.

Reed-Solomon Decoder

Integrated Silicon Systems
See profile on page 70.

Applications

- Buses & Interfaces
- Processor & Peripherals
- ✓ Telecom & Datacom
- DSP for Imaging
- ✓ DSP for Communications

- Parameterized error correction coding (ECC)
- Variable decoding rate option
- Highly optimized architecture
- Capable of high speeds (> 400 megabits per second)
- Applications include:
  - Digital video broadcast (DVB)
  - Digital audio broadcast (DAB)
  - Digital satellite broadcast
  - High-speed modems
  - Compressed audio and video for CATV, HDTV, and DBS

The Reed-Solomon decoder megafunction incorporates high functionality, ease of use, and an optimized architecture to produce a design that fits into the FLEX 10K and FLEX 8000 devices.

Designers can choose between fixed or variable decoding rates. With a variable decoding rate, a single Reed-Solomon decoder megafunction can handle decoding in systems with large variations between the signal-to-noise ratios of their channels.

ISS can customize the megafunction to meet specific application requirements. Customizable parameters include the number of bits per symbol and error handling rate.

ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K						Q1 1997
FLEX 8000						Consult Partner
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

Reed-Solomon Encoder

Integrated Silicon Systems
See profile on page 70.

Applications

- Buses & Interfaces
- Processor & Peripherals
- ✓ Telecom & Datacom
- DSP for Imaging
- ✓ DSP for Communications

- Parameterized error correction coding (ECC)
- Variable encoding rate option
- Highly optimized architecture
- Capable of high speeds (> 400 megabits per second)
- Applications include:
  - Digital video broadcast (DVB)
  - Digital audio broadcast (DAB)
  - Digital satellite broadcast
  - High-speed modems
  - Compressed audio and video for CATV, HDTV, and DBS

The Reed-Solomon encoder megafunction incorporates high functionality, ease of use, and an optimized architecture to produce a design that fits into FLEX 10K and FLEX 8000 devices.

Designers can choose between fixed or variable encoding rates. With a variable encoding rate, a single Reed-Solomon encoder megafunction can handle encoding in systems with large variations between the signal-to-noise ratios of their channels.

ISS can customize the megafunction to meet specific application requirements. Customizable parameters include the number of bits per symbol and error handling rate.

ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K	EPF10K10	-3	208	0	54 MHz	Available Now
FLEX 8000						Consult Partner
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example has 8 bits per symbol, a block size of up to 255 symbols, and 8 symbol errors per block.

Speedbridge

SIS Microelectronics
See profile on page 67.

Applications

- Buses & Interfaces
- Processor & Peripherals
- ✓ Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- Elastic FIFO for bridging data between various speed domains
- Customized widths and depths
- Provides full/empty status flags
- Independently clocked input and output interfaces
- Register based

The Speedbridge megafunction is a speed-matching FIFO buffer that transfers data across an asynchronous interface. The read and write ports have independent clocks and synchronous enables for accessing their respective functions. These features allow the clocks to run without read or write operations occurring.

The megafunction eliminates the need for an external asynchronous FIFO, which helps minimize system development and debugging time and reduce development cost and risk in design. SIS Microelectronics can customize the megafunction's width and depth according to user specifications.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Notes (2), (3)*	EPF10K10	-3	256	0	62 and 45 MHz	Available Now
FLEX 8000, *Notes (2), (3)*	EPF8452A	A-2	256	–	62 and 50 MHz	Available Now
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) Implementation shown has four 32-bit words.
(3) The performance (f_{MAX}) calculations shown are for write and read clocks, respectively.

Square Root Operator

Integrated Silicon Systems
See profile on page 70.

Applications

- Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- ✓ DSP for Imaging
- ✓ DSP for Communications

- Fully parameterized megafunction
- High performance
- Small size
- Applications include:
  - Digital signal processing
  - Control processing
  - Data processing

When used with other mathematical operators, the square root operator megafunction allows complex systems and calculations to be implemented in programmable logic and accelerates calculation operations by orders of magnitude.

ISS can customize the performance and data word length and format to meet specific application requirements. ISS provides test vectors, full documentation, and technical assistance to help designers embed the megafunction into their projects.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K, *Note (2)*	EPF10K50	-3	1,019	0	33.33 MHz	Available Now
FLEX 8000	–	–	–	–	–	–
MAX 9000	–	–	–	–	–	–
MAX 7000	–	–	–	–	–	–

Notes:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) This example has a 16-bit radicand, 16-bit square root, and pipelining = 18 (maximum pipelining = 18).

XMIDI Modular UART Library

Digital Design Development
See profile on page 64.

Applications

- ✓ Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- Fully compatible with musical instrument digital interface (MIDI)
- Most flexible macro set for eXtended-MIDI (XMIDI) implementation
- Runs up to 32 times MIDI speed
- Highly reconfigurable

The XMIDI modular UART library contains a set of building blocks that are used in XMIDI communications applications. The megafunctions allow easy expansion to any number of receiver and transmitter channels, FIFO depths, and complementary functions (e.g., parser).

The library includes the following modules: a binary coded ternary (BCT) transmitter and receiver (both with XM channel encoding/decoding), cascadable clock dividers, a 17-bit wide FIFO slice or FLEX 10K EAB FIFOs, and a fully static XM operand encoder/decoder.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K	EPF10K10	Any	*Note (2)*	2 (Min.)	32 MHz	Consult Partner
FLEX 8000	EPF8452A	Any	*Note (2)*	–	32 MHz	Consult Partner
MAX 9000	EPM9320	Any	*Note (2)*	–	32 MHz	Consult Partner
MAX 7000	–	–	–	–	–	–

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.
(2) Megafunction sizes vary. Contact the partner for an LC count that is based on user specifications.

XM-01 XMIDI Basic UART

Digital Design Development
See profile on page 64.

Applications

- ✓ Buses & Interfaces
- Processor & Peripherals
- Telecom & Datacom
- DSP for Imaging
- DSP for Communications

- Fully compatible with musical instrument digital interface (MIDI)
- Smallest macro set for eXtended-MIDI (XMIDI) implementation
- Runs up to 8 times MIDI speed
- Bidirectional line handling
- Four different bus modes to fit any MCU or CPU

The XM-01 XMIDI basic UART megafunction is a minimal-size implementation of a double-buffered send and receive XMIDI UART. For full bidirectional capability, a second XMIDI UART is required. The host MCU or CPU handles the extended operand coding/decoding.

The megafunction includes the following features: a binary coded ternary (BCT) transmitter and receiver, bit mapping for channel encoding and decoding, and line control and sensing on both the data and through outputs. The megafunction assures line coherency, and has dual clock dividers that allow independent baud rates for RX and TX channels up to 250 Kbaud rate. Polling and interrupt modes are also possible.

Size & Performance Information *Note (1)*

Device Family	Smallest Target Device	Speed Grade	Device Utilization		Performance (f_{MAX})	Availability
			LCs	EABs		
FLEX 10K	EPF10K10	Any	226	0	8 MHz	Available Now
FLEX 8000	EPF8452A	Any	226	–	8 MHz	Available Now
MAX 9000	EPM9320	Any	127	–	8 MHz	Available Now
MAX 7000	EPM7128E	Any	122	–	8 MHz	Available Now

Note:
(1) Specifications are subject to change. See page 11 for more information regarding this table.

AMPP Partner Profiles

February 1997

Overview

The AMPP partner profiles contain contact, background, and historical information on each partner company that is currently participating in AMPP. Each partner profile has a list of available products and may include a description of available services. Not all megafunctions listed in the partner profiles are available for Altera device architectures. Contact the appropriate AMPP partner for information on products, availability, pricing, and delivery terms.

CAST, Inc.

24 White Birch Drive
Pomona, NY 10970
Tel. (914) 354-4945
Fax (914) 354-0325

info@cast-inc.com
http://www.cast-inc.com

Overview

CAST focuses on maximizing the success of PLD designs by supplying high-quality, high-value megafunctions for simulation and synthesis. CAST provides a total modeling solution for PLD design by delivering and supporting VHDL libraries with thousands of accurate, reliable, and affordable functions ready for use by designers worldwide. CAST supplies maintenance and support programs, including a models on request (MOR) service, as well as a variety of VHDL training programs and consulting services.

CAST pre-packaged libraries feature Standard Component VHDL Library (SCVL) series. Developed for system and device designers, SCVL includes simulation models for 3,000 memory devices and 2,500 standard ECL and TTL devices.

The V-Custom Series library provides affordable VHDL megafunctions such as processors, complex functions, and specialized devices. The library currently includes in-stock models such as the Pentium and Pentium Pro processors from Intel and a variety of network and memory controllers, coprocessors, and timers. Check the CAST world-wide web page for information on newly added megafunctions.

If a megafunction is not currently available, CAST can create custom megafunctions on request. The CAST experts work closely with designers to produce the exact megafunctions required, from complex processor functions to specialized peripheral devices. CAST delivers the best available combination of up-front economy, long-term value, and personalized support.

Available Products

CAST provides the megafunctions and simulation models summarized in the following table. Not all products are available for Altera devices. Contact CAST for availability.

Megafunction	Description
C_UART	Generic UART
C2910	Microprogram controller
C49410	Microprogram controller
C6850	UART
C68450	DMA controller
29116	Microprocessor
8031/8051	Controller
8085	Microprocessor
8203	64K dynamic RAM controller
8237/8257	Programmable DMA controller family
8253	Programmable interval timer
8254	Programmable interval timer
8255A	Programmable peripheral interface
8259A	Programmable interrupt controller
82586	Local area network coprocessor
82596	Local area network coprocessor

Digital Design & Development

18A Godshuis Street, 1861
Meise, Belgium
Tel. (32) 2-270-2797
Fax (32) 2-270-1905

73261.530@compuserve.com
http://ourworld.
compuserve.com/homepage
s/eric_lukac_kuruc/ddd.htm

Overview

Digital Design & Development (DDD) produces eXtended MIDI (XMIDI) megafunctions, an improved version of the MIDI communication system. XMIDI uses both hardware and software to overcome the limitations of traditional MIDI systems, while remaining completely compatible with existing MIDI systems.

XMIDI upgrades conventional MIDI in two ways:

- Expanding traditional MIDI functions and capabilities
- Adding numerous new functions

DDD provides the expertise to assist designers in understanding XMIDI and integrating the system's functions in custom products.

Available Products

DDD provides the megafunctions and products summarized in the following table. Not all products are available for Altera devices. Contact DDD for availability.

Megafunction	Description
XM-DEV	XMIDI development board
XM-PC	ISA-PC to XM-DEV interface board and software
XM3V710	XMIDI programmed EPM7128E
XM-01	Basic XMIDI function
XM-Blocks	Modular function system for XMIDI implementation

Eureka Technology, Inc.

4962 El Camino Real
Suite 108
Los Altos, CA 94022
Tel. (415) 960-3800
Fax (415) 960-3805

info@eurekatech.com

As design cycles become shorter, time-to-market is critical for a successful development project. Every product must meet aggressive design goals with limited resources and tight schedules. Eureka Technology provides sophisticated design capabilities to assist logic designers. By offering reusable megafunctions, custom design services, and simulation models for PLD and ASIC designs, Eureka Technology can help designers reduce costs and shorten design times to meet time-to-market demands.

Eureka Technology supplies products for the computer, communications, and semiconductor industries, and offers megafunctions in the following areas:

- PowerPC bus controller functions
- PCI bus controller functions

These functions are designed to handle complex PowerPC and PCI bus systems, and to provide a simple, efficient interface to the user's internal design. Designers can use these megafunctions to reduce design costs and quickly master the PowerPC and PCI bus systems.

The designer can parameterize Eureka Technology megafunctions for specific system requirements. In addition, Eureka Technology can provide user-specified features on request. By offering customized design services, Eureka Technology can quickly expand the user's design capabilities to meet market demands.

To be successful, complex systems must be evaluated effectively before being committed to silicon. Not only should each individual ASIC be verified through functional simulation, but system-level simulation should also be an integral part of the design process. Eureka Technology offers simulation models as well as megafunctions to help system designers verify every aspect of their systems before silicon implementation.

Eureka Technology design engineers have a wide variety of design expertise and are knowledgeable in many design areas, including:

- PLD and ASIC design
- PowerPC bus systems
- PCI bus systems
- PC architecture and chip set
- Cache and memory controllers
- CPU and embedded controller megafunctions
- Specialized memory devices

Eureka Technology provides support for the following IC development phases:

- Top-down design methodologies
- Behavioral modeling
- Synopsys logic synthesis
- PLD and ASIC implementation
- VHDL and Verilog HDL simulation
- Functional verification

Excellent Design Inc.

2-3-19, Shinyokohama
Kouhoku-ku
Yokohama-Shi, Kanagawa,
222 Japan
Tel. (81) 45-474-9410
Fax (81) 45-474-9413

ampp@exd.co.jp

Overview

Excellent Design Inc. supports semiconductor vendors and ASIC developers with VLSI design and advanced EDA tool development. Excellent Design provides high-performance, high-quality VLSI designs and development environments using the knowledge of ASIC designers, system architecture engineers, and EDA tool engineers. Excellent Design is also a worldwide supplier of application-specific standard products (ASSPs) and EDA tools for ASIC-based technologies.

Reusability is an important goal in design and architecture development, and is the main purpose of process-independent design. To achieve this goal, Excellent Design employs the top-down design methodology commonly used in device system design. Excellent Design is also researching and developing a cell library that can be mapped to different device processes and architectures.

Excellent Design uses a "bottom-up oriented top-down" method, in which a circuit is synthesized from its behavioral description (top-down) while physical layout for the circuit is mapped on the target process (bottom-up) to complete the library. This method is useful for fabless integrated circuit designers.

Excellent Design provides the following products and services to support all aspects of custom circuit development:

- Strong relationships with international companies who supply advanced architectures
- Original ASSP devices
- Advanced design environment and libraries
- ASIC vendors and users by combining EDA tools, system, and software technologies

Available Products

Excellent Design provides the megafunctions summarized below. Not all products are available for Altera devices. Contact Excellent Design for availability.

CPU Megafunctions

- Z80-compatible CPU

CPU Peripherals

- 8237-compatible DMA controller
- 8251-compatible serial interface
- 8254-compatible timer and counter
- 8255-compatible parallel interface
- 8259-compatible interrupt controller
- 16550 compatible high-speed serial interface
- PCI bus interface model

Future Products

- IrDA interface
- HDLC controller
- NTSC/PAL Digital Video Encoder
- DCT engine

FASTMAN, Inc.

1613 Capitol of TX Hwy S.
Suite 222
Austin, TX 78746
Tel. (512) 328-9088
Fax (512) 328-9317

mrt@fastman.com
http://www.fastman.com

Overview

FASTMAN, Inc. develops data compression products featuring high compression rates that still maintain data quality and integrity. FASTMAN's megafunctions are based on the proprietary Adaptive Wavelet Transform (AWT) techniques, which exceeds the data-compression and quality performance of current-generation compression methods. The megafunctions are used in high-data-fidelity, high-speed data compression applications with low-bandwidth communications channels.

FASTMAN also holds several patents in data compression. RapidTransit, a software-only version of the AWT technique, delivers high-quality audio products within the evolving internet standards for communication and application interfaces.

Available Products

FASTMAN currently provides the following megafunctions:

- *Biorthogonal wavelet filter*—Integrated low-pass and high-pass biorthogonal wavelet filter. The 16-bit input data is clocked at 50 MHz; output data consists of alternating low-pass and high-pass data at 25 MHz each. This megafunction is optimized for Altera's FLEX 10K devices.
- *Decimating digital filter*—Typical data input rate is 100 MHz. The filter can have 3 to 24 taps and can support an odd or even number of taps. It also has 4-, 8-, 16-, or 32-bit data samples.

FASTMAN plans to introduce megafunctions for DSP applications. Future products include FFT, DCT, and image filtering megafunctions. Contact FASTMAN for more detailed information.

Integrated Silicon Systems, Ltd.

29 Chlorine Gardens
Belfast, BT9 5DL,
Northern Ireland
Tel. (44) 1232-664-664
Fax (44) 1232-669-664

info@iss-dsp.com
http://www.iss-dsp.com

Overview

Integrated Silicon Systems is a DSP intellectual property company specializing in synthesizable DSP products. ISS has an acknowledged worldwide competence in VLSI architectures for DSP and supplies highly optimized DSP circuit functions for ASIC and CPLD implementation.

The key advantages of using ISS products are:

- Highly efficient silicon implementations after synthesis
- Dramatically reduced design times for rapid prototyping and fast time-to-market
- Very high performance—orders of magnitude greater than programmable DSP cores
- Characterized for the world's principal fabrication processes

ISS's main products are:

- *DSP ASIC library*—A comprehensive library of parameterized, synthesizable DSP building blocks written in VHDL. Over 170 blocks are contained in the library and include multipliers, dividers, square root operators, adders, accumulators, counters, and data format converters, available in a number of fixed- and floating-point formats.
- *DSP function-level cores*—An extensive range of highly parameterized DSP function-level blocks for efficient ASIC and CPLD implementation. Typical blocks include FIR filters, Reed-Solomon encoders and decoders, adaptive filters, FFT, DCT, IIR filters, median filters, and front-end image processing functions.
- *DSP system-level cores*—A range of parameterized system-level blocks including high performance JPEG and multi-channel ADPCM codecs for efficient ASIC and CPLD implementation.

All blocks are fully parameterized, allowing the ultimate in design flexibility and design reuse. ISS's range of megafunctions is optimized for Altera CPLDs, giving Altera customers a unique advantage in the CPLD-based design of complex systems.

Available Products

ISS optimizes its cores and library blocks for Altera CPLD implementation and provides full technical support. A list of typical megafunctions available from ISS for Altera FLEX 10K and FLEX 8000 implementation are shown in the table below. Contact ISS for more information on specifications and availability.

Products		Description
System level	JPEG	High-performance JPEG encoders and decoders.
	ADPCM	Supports 6 ITU ADPCM standards with multi-channel capability.
Function level	FFT	High performance FFTs in 16-, 64-, and 256-point formats.
	DCT	DCT, IDCT, and combined DCT/IDCT blocks for 8 × 8 2-D DCT operation.
	Reed-Solomon	High-performance Reed-Solomon encoders and decoders.
FIR filter library		A comprehensive FIR filter capability to produce highly customized and high-performance FIR filters.
IIR filter library		A comprehensive IIR filter library for custom IIR filters.
Adaptive filters		Includes LMS filter and custom adaptive filtering.
Image processing library		High-performance front-end image processing functions including edge detectors and image enhancement filters.
Rank order filters		1-D and 2-D variants including programmable filters and median filters.
Arithmetic operators		Includes multipliers, dividers, square root operators, adders, and data format converters. All available in fixed- and floating-point formats.

KTech Telecommunications, Inc.

15501 SF Mission Blvd.
Suite 100
Mission Hills, CA 91345
Tel. (818) 361-2248
Fax (818) 270-2010

skuh@ktechtelecom.com
http://www.ktechtelecom.com

KTech Telecommunications, Inc. is an ASIC design service company with experience in the following digital ASIC products:

- 8- and 16-bit VSB demodulators for ATSC "Grand Alliance" signal
- Decision feedback equalizer
- Trellis coded modulation (TCM) decoder
- 2 channel GPS base and processor

KTech offers the following megafunctions for use in modulator/demodulator communications products:

- Convolutional interleaver
- QPSK burst demodulator
- Bit synchronizer
- Carrier synchronizer
- Automatic gain control

Logic Innovations, Inc.

6205 Lusk Boulevard
San Diego, CA 92121
Tel. (619) 455-7200
Fax (619) 455-7273

info@logici.com
http://www.logici.com

LOGIC INNOVATIONS

Overview

Logic Innovations, Inc. is a turn-key engineering development firm that has developed over 500 systems for OEM release and custom, industrial use. Logic Innovations products are used in the following applications:

- PCI, ATM, PCMCIA, EISA, and ISA computers
- Set-top boxes
- Hand-held and laptop computers
- MPEG-2 systems
- Cable TV and DSS/DVB TV systems
- Cable TV test equipment
- Wireless communications
- In-flight entertainment systems for commercial aircraft
- Supercomputers
- Laser printers
- Industrial environments such as VME and multi-bus

Logic Innovations' PCI and ATM megafunctions are optimized for maximum performance and minimal silicon costs. PCI megafunctions allow designers to implement designs requiring a PCI bus master or target interface, and ATM megafunctions allow designers to implement designs requiring ATM transmission convergence sublayer functions. The PCI and ATM megafunctions are silicon-proven cores, and are implemented in VHDL and Verilog HDL. Netlist versions of the megafunctions synthesized for specific target devices are available for applications that do not require source code modification.

These megafunctions are developed using Logic Innovations' product development experience. This approach differs from "model farms" where software engineers create megafunctions from specifications. These megafunctions derive from real-world applications created by experienced hardware and device designers.

Logic Innovations' megafunctions are verified in working products before being released to designers. The megafunctions use architecture-specific constraints and constructs as required for optimized routing. The synthesized megafunctions are efficient, require minimal gate count, and provide full-speed operation.

Logic Innovations provides the following competitive advantages:

- Technology-driven, expert design solutions
- Low-cost VHDL and Verilog HDL design files
- Optimized models for programmable logic
- Fully documented design files and manuals
- Evaluation boards
- Model customization services
- Turn-key hardware and software development services
- Ten-year record of satisfied customers

Available Products

Logic Innovations provides the products summarized below. Not all products are available for Altera devices. Contact Logic Innovations for availability.

PCI Bus

- 64-bit PCI bus master/target
- 32-bit PCI bus master/target
- 32-bit PCI bus target

ATM

- Transmission convergence cell inlet model
- Transmission convergence cell outlet model
- Transmission convergence cell inlet/outlet model
- UTOPIA level 2 interface building blocks
- Broadband cell delineation building blocks

Logic Innovations' PCI and ATM megafunctions are provided as design kits that include the VHDL or Verilog HDL source code, test bench, and complete documentation.

Nova Engineering, Inc.

5 Circle Freeway Drive
Cincinnati, OH 45246-1105
Tel. (513) 860-3456
Fax (513) 860-3535

info@nova-engr.com
http://www.nova-eng.com

Overview

Nova Engineering, Inc. specializes in the design and development of leading-edge communications and signal processing systems. Nova has comprehensive experience in military, government, and commercial electronics, with an emphasis on state-of-the-art digital communications systems. Nova's innovative solutions have resulted in numerous patents and a series of successfully deployed communications and signal processing systems.

Nova provides design services that support the total communication systems development cycle. The cycle begins with innovative communications system engineering, followed by extensive analysis and computer simulation, including simulation software developed by Nova. Reducing system designs to hardware draws upon Nova's extensive expertise in miniature, low-power radio frequency (RF), including handheld transceivers, high-performance modems, and ultra-low phase noise synthesizers. Included in Nova's designs are low-noise RF amplifiers, frequency agile filters, wide-range VCOs, and even custom antennas, spanning the range from HF through microwave frequencies.

Embedded real-time signal processing, PLDs, and ASICs play a major role in virtually every Nova product. The signal processing techniques are as diverse as forward error correction (e.g., BCH, Reed-Solomon, and Nadler functions), Kalman filters, digital modulation/demodulation and low-rate, toll-quality vocoders. Nova's experience in communication product design has led to rapid prototyping using VHDL and PLDs to take advantage of the value provided by programmable logic and module re-use.

PLD Solutions

Nova's PLD solutions have the following advantages:

- *Improved system throughput*—Implementing processing algorithms in PLDs as separate co-processors or pre-processors substantially improves system performance. Algorithms can be designed to execute in parallel, providing valuable gains in processing throughput.
- *Rapid prototyping*—PLDs can circumvent and complement long ASIC design cycles. The combination of PLDs and megafunctions accelerates hardware development, leaving the designer free to evaluate and improve the design. With PLDs, designers can evaluate and implement design changes in hours instead of months.

- *Design optimization*—PLDs can shrink board space, reduce power, and improve system reliability because multiple integrated circuits can be consolidated into a single PLD. Reducing a multi-device solution to a single PLD allows the design to be optimized for size, power, performance, and cost.
- *Real-time adaptability*—Designers can realize significant space, weight, and cost savings by using one device for multiple functions. PLDs with in-circuit reconfigurability (ICR) or in-system programmability (ISP) permit design changes to be implemented "on-the-fly" and in the field.

Available Products

Nova provides the communications megafunctions listed below. Not all megafunctions are available for Altera devices. Contact Nova Engineering for availability.

- Numerically controller oscillators (NCO)
- Complex mixers
- Digital modulators and demodulators (AM, FM, PSK, FSK, and QAM)
- Data synchronizers
- Binary pattern correlator
- Custom FIR filters
- PN code generators

Phoenix Technologies, Ltd.

411 East Plumeria Drive
San Jose, CA 95134
Tel. (408) 570-1000
U.S. (888) 4VCHIPS
Fax (408) 570-1230

sales@vchips.com
http://www.phoenix.com

Overview

The Virtual Chips division of Phoenix Technologies, Ltd. develops and markets synthesizable cores and test environments for computer-industry standards including PCI, USB AGP, CardBus, and PCMCIA. Simulation models for speciality memories are also available.

Portfolio Features & Benefits

The Virtual Chips product line is developed and maintained by experienced system designers. All products include the features, documentation, and support necessary to ensure a smooth integration into customer designs. Products are available in both Verilog HDL and VHDL formats.

The Virtual Chips application-optimized PCI cores are designed to ensure optimal system throughout and full PCI performance at 33 or 66 MHz. The cores are silicon-proven, and they have been verified in a wide range of applications by an installed base of over 100 customers. The Virtual Chips PCI Bus test environment includes bus models, a PCI compliance test suite, and a set of macro commands to create a realistic system simulation environment for PCI.

The Virtual Chips USB development solution includes the following components for a designer to create USB-compatible systems, peripherals, and chips:

- Synthesizable cores for USB host, hub, and function
- The Virtual Chips USB test environment
- USBWorks, a Windows 95 application that allows end users to configure devices, diagnose bus-related problem, and monitor bus bandwidth usage
- The Phoenix BIOS USB extensions
- USB development platform that integrates PLDs and software for USB peripheral design

Available Functions

Phoenix Technologies provides the Virtual Chips products summarized below. Not all products are available for Altera devices. Contact Phoenix Technologies for availability.

PCI Products

- PCI satellite cores—Available in 32-bit and 64-bit PCI and application interface configurations, asynchronous or synchronous, with or without FIFOs, and 33 MHz or 66 MHz operation.
- PCI host bridge cores—Available in 32-bit and 64-bit PCI and application interface configurations, asynchronous or synchronous, with or without FIFOs, 33 MHz or 66 MHz operation.
- PCI bus test environment

USB Products

- USB host, hub, and function synthesizable cores
- USB test environment
- USBWorks utility application
- Phoenix BIOS USB extension
- USB development platform

PC Card Products

- 32-bit cardbus test environment
- 16-bit PCMCIA test environment

Speciality Memory Simulation Models

- Fujitsu: 16M SDRAM
- Hitachi: 4M SDRAM, 8M SGRAM, 16M SDRAM, and 64M SDRAM
- IBM: 16M SDRAM and 16M ESRAM
- NEC: 8M SGRAM, 16M SDRAM, 16M EDO DRAM, 16M/18M Rambus DRAM, Rambus ASIC Cell (RAC), 64M 2/4 bank SDRAM, and SDRAM DIMM
- Oki: 2Mx8 SDRAM
- Toshiba: 16M SDRAM (Verilog HDL)

Richard Watts Associates, Ltd.

8 Church Square
Leighton Buzzard,
Bedfordshire
LU7 7AE
England, UK
Tel. (44) 0 1525 372621
Fax (44) 0 1525 383228

coreinfo@evolution.co.uk
http://www.evolution.co.uk/rwa

Overview

Richard Watts Associates (RWA) specializes in designing MegaCell functions for PLD and ASIC technologies, which help designers meet the goals of high performance, lower cost, and faster time-to-market. RWA has ten years of design experience with real-time embedded system software for many different processors and DSPs, including the 8052. The company can also support customers in any form of product development.

RWA supplies ready-made MegaCell functions for standard part replacement and multimedia applications. The functions are designed in VHDL, which makes them independent of EDA tool and process. Individual functions are available as behavioral VHDL, dataflow VHDL, dataflow Verilog HDL, and process optimized blocks. MegaCell functions are supplied with high-fault coverage test vectors.

All of RWA's MegaCell functions are fully synchronous and static designs. Modern design techniques have been used to enhance performance and reduce area. Many functions are supported with extra models to aid system design such as in hardware and software co-simulation debuggers. All MegaCell designs can be customized by RWA or the designer.

Available Products

RWA provides the megafunctions summarized below. Not all products are available for Altera architecture devices. Contact RWA for availability.

CPU MegaCell Functions

- RAW8031/51 accelerated 8-bit microcontroller
- RAW8032/52 accelerated 8-bit microcontroller
- BARECORE accelerated 8-bit CPU
- RAW8031/51-A Altera-optimized, accelerated 8-bit microcontroller
- RAW8032/52- A Altera-optimized, accelerated 8-bit microcontroller
- BARECORE-A Altera-optimized, accelerated 8-bit CPU

Multimedia MegaCell Functions

- Soundgun
- Globalizer

The Soundgun MegaCell function is a 16-bit PCM high-performance music synthesizer with effects and downloadable sample support. It has 128 general MIDI sounds with up to 48-voice polyphony, with a second order resonant digital filter to further enhance the sound. A spatial sound enhancer is part of the standard package. Legacy sound card requirements are also supported. The Soundgun MegaCell function comes with a sample ROM set, firmware for a full general MIDI sound set, and general standard drum sounds. The MegaCell functions are available in PCI or AT bus versions.

The Globalizer MegaCell function is a stereo effects processor with reverb, chorus, echo, and spatial effects. This function is suitable for increasing the number of digital audio products for the consumer market. The Globalizer MegaCell function will integrate new advanced features into products such as digital TV, CD players, Karaoke, Hi-Fi, and car radios.

Sand Microelectronics, Inc.

3350 Scott Boulevard
Suite 24
Santa Clara, CA 95054
Tel. (408) 235-8600
Fax (408) 235-8601

sales@sandmicro.com
http://www.sandmicro. com

Overview

Sand Microelectronics, Inc. provides IP and related tools for industry-standard interfaces such as PCI and USB. Sand's comprehensive IP solutions are compatible with the SANDesigner ADVantage Solutions, which include analysis, design, and verification (ADV) tools. These solutions allow designers to integrate projects quicker and more efficiently, which improves time-to-market and design integration.

Sand's analysis tools permit designers to optimize megafunction performance during simulation. With RapidScript, designers can configure the megafunctions to meet optimal requirements without changing the source code of the function.

Available Products

Sand provides the products listed below. Not all products are available for Altera devices. Contact Sand Microelectronics for availability information.

Verilog HDL & VHDL Simulation Models

- PCI bus model
- PCI compliance test suite
- USB model
- DRAM, SDRAM, SGRAM models

Silicon-Proven Cores (Available as Netlists, Verilog HDL & VHDL)

- PCI with RapidScript—The designer can implement 32 configurations for each megafunction.
  - PCI 32-bit, 33-MHz, 32-, and 64-bit application, synchronous/asynchronous FIFO function
  - PCI 64-bit, 33-MHz, 32-, and 64-bit application, synchronous/asynchronous FIFO function
  - PCI 64-bit, 66-MHz, 32-, and 64-bit application, synchronous/asynchronous FIFO function
- USB device controller (UDC) with RapidScript—The designer can optimize the function for applications such as digital cameras, scanners, modems, keyboards, audio, and printers.
- USB host controller, OMCI compliant
- USB hub controller, supports 2 to 15 downstream ports

Performance Analyzers

The following performance analyzers enable designers to optimize performance prior to silicon fabrication:

- PCI performance analyzer
- USB analyzer

Sierra Research and Technology, Inc.

6035 Kerrmoor Drive
Westlake Village, CA 91362
Tel. (818) 991-1509
Fax (818) 991-1508

cores@srti.com

Overview

Sierra Research and Technology, Inc. (Sierra) was incorporated in February 1993, and is headquartered in Mountain View, California. The three founders have more than 50 years of experience in engineering and management positions at some of Silicon Valley's largest and most successful companies. The technical staff at Sierra is a responsive, educated group of engineers that are well-suited to tackle advanced design projects.

From concept to silicon, Sierra offers standard designs and custom design services for networking, data communications, CPU megafunctions, and storage devices. Sierra supports customer-initiated projects, including complex systems, analog circuits, mixed analog-digital design, and digital circuit design.

Sierra provides device, board, and system designs for semiconductor, systems, and peripherals companies. Licensed semiconductor companies can manufacture and distribute Sierra's 622-Mbs ATM and 100-Mbs Ethernet. Currently, Sierra is developing several CPU megafunctions from the 68*xx* and R3*xxx* families.

With a variety of EDA tools for simulation, synthesis, and layout, Sierra can perform layout for gate array, standard cell, or custom device methodologies. Sierra also provides access to leading-edge prototyping, (e.g., building limited quantities of large devices that run at speed in the final package). This process aids system houses and other designers who require engineering samples before first device fabrication.

The combination of independent verification engineers, state-of-the-art EDA tools, and leading-edge prototyping has enabled Sierra to complete more than two dozen chip designs on time and according to specifications. Most designs were completed without a single chip revision cycle.

With megafunctions, designers save money, improve time-to-market, and are assured high-quality designs. Sierra uses the latest EDA design tools and methodology to ensure that designs work correctly the first time.

Available Products

Sierra provides the megafunctions summarized below. Not all products are available for Altera devices. Contact Sierra for availability.

- S68*xx* —68*xx* CPU megafunctions
- SR3*xxx*—MIPS R3*xxx* CPU megafunctions
- Fast Ethernet controller—10- to 100-Mbs Ethernet controller for PCI to MII bus
- Fast Ethernet PHY—10- to 100-Mbs TX physical
- Fast Ethernet MAC—10- to 100-Mbs ethernet MAC
- OC12 ATM SAR—622-Mbs ATM segmentation and reassembly

Silicon Engineering, Inc.

269 Mt. Hermon Road
Suite 101
Scotts Valley, CA 95066
Tel. (408) 438-5330
Fax (408) 438-8509

info@sei.com
http://www.sei.com

SILICON ENGINEERING, INC.

Silicon Engineering, Inc. (SEI) provides custom and semi-custom IC design capability and technology licenses for the systems, semiconductor, and consumer electronics industries.

For the past decade, SEI has applied system knowledge and design expertise to a variety of application areas, including super-integrated graphics and multimedia chipsets, disk drive controllers, memory controllers, RAMDACs, high-speed SRAM, networking chipsets, embedded controllers, and consumer game controllers. Designs range in complexity from 10,000 to 2 million gates. Recent projects include a 3-dimensional graphics controller, 64-bit RISC CPU, 200-MHz RAMDAC, 5-ns embedded dual-port SRAM, 3-V disk controller, GUI accelerator, laser printer engine, Ethernet controller, and an audio device. SEI can use a range of information as the starting-point for new designs—from marketing requirement documents to pre-existing designs requiring modification.

SEI utilizes industry-standard methodologies and tools from Cadence, Synopsys, Viewlogic, and Mentor Graphics to match the designer's environment. A top-down and well-structured design methodology is followed throughout the design cycle in order to minimize design time and ensure first-pass success. Using industry-standard tools augmented with proprietary tools enables SEI to rapidly design ASICs and ASSPs implemented in gate array, standard cell, or high-density PLDs. SEI can then convert these same designs to full, custom ICs for production quantities.

SEI implements designs for any performance level or production volume. Depending on the device specification and marketing requirements, SEI can recommend the most appropriate implementation device.

SEI has the following systems expertise:

- Two-dimensional and three-dimensional (2-D/3-D) imaging
- Graphics chipsets
- High speed RAMs and DACs
  - RAMDAC
  - DAC, ADC, PLL
  - SRAMs
- Communications chipsets
  - Ethernet
  - ATM

- Storage chipsets
  - Disk controller
  - Motor controller
- Consumer chipsets
  - IR-based communication
  - Voice recognition and synthesis

The following licenses are available:

- AMPP megafunctions
- Verilog HDL megafunctions
- Full custom megacells
- EDA point tools
- Standard cell libraries
- Memory arrays

SEI offers the following services:

- Gate array and standard cell design
- Full custom and layout design
- Technology conversions
- EDA tools and library development
- Mixed analog/digital design
- PLD design

SIS Microelectronics, Inc.

1831 LeftHand Circle
Suite E
P.O. Box 1432
Longmont, CO 80501

Product Information:
Tel. (303) 776-1667 x223
Fax (303) 776-5947
info@sismicro.com

Technical Support:
Tel. (303) 776-1667 x226
Fax (303) 776-5947
support@sismicro.com

Overview

SIS Microelectronics, Inc. (SIS) was founded in 1982 on the principle that, to be successful in the electronics marketplace, a partnership between the system designer and the chip maker is essential. The SIS proven team approach provides its partners with the equivalent of an "in-house" chip supplier. SIS supports the system development process from concept to customer delivery.

SIS supplies silicon solutions for the embedded-processor market. SIS is currently shipping three "off-the-shelf" ASICs that reduce the cost and time-to-market of laser printers. The most recent product is the SFBC-licensed memory compression from Adobe Systems, Inc.

SIS provides a variety of megafunctions, including ASSPs, IC megafunctions, processor interfaces, and laser printer engine drivers.

Available Products

SIS provides the megafunctions summarized below. Not all products are available for Altera devices. Contact SIS for availability.

Silicon-Proven IC Megafunctions (Available for Altera Devices)

- *Speedbridge*—Elastic FIFO for bridging data between speed-variant domains
- *IEEE 1284 Parallel Slave Interface*

Application-Specific Standard Products (ASSPs)

- *SMEMC*—Highly integrated memory/peripheral controller
- *SLPC*—Peripheral controller for laser printer applications
- *SFBC*—Adobe-licensed frame buffer compression (memory reduction for laser printers)

Processor Interfaces

- IEEE 1284 parallel slave interface
- VR4300
- Intel 960C*x*/J*x*
- IDT Orion
- AMD 29030/040
- DMA controller
- DRAM controller
- ROM/SRAM controller

Laser Printer Engine Printer Drivers

- Timer/counter
- Interrupt controller
- 450/550 UART
- IEEE 1284 parallel slave interface
- RLE compression engine
- 32-bit multiplier
- Serial EEPROM interface

Synova, Inc.

1333 Gateway Drive
Suite 1017
Melbourne, FL 32901
Tel. (407) 728-8889
Fax (407) 728-9587

ampp@synova.com

Overview

Synova is a commercial fabless semiconductor company that specializes in accelerated integrated circuit development cycles using core-based design techniques. Synova's complex cores enable incorporation of digital video and embedded RISC microprocessor designs into systems-on-a-chip. Synova's core-based design methodology provides decreased time-to-market solutions for ASIC-based products. Synova's core products developed for ASICs are available as sophisticated megafunctions for PLDs.

Available Products

Synova provides the megafunctions summarized below. Not all products are available for Altera devices. Contact Synova for availability or check Synova's web site.

The current megafunctions include:

- JPEG encoder
- JPEG decoder
- MPEG II decoder
- IEEE-754 floating-point function
- High-performance Fast Fourier transform function

Synova also offers radiation-hardened standard products which include:

- 32-bit MIPS microprocessor
- 32-bit MIPS microcontroller core-based ASIC
- Peripheral interface controller

VAutomation, Inc.

20 Trafalgar Square
Suite 443
Nashua, NH 03063
Tel. (603) 882-2282
Fax (603) 882-1587

ampp@VAutomation.com
http://www.vautomation.com

Overview

VAutomation's synthesizable hardware description language (HDL) megafunctions provide designers with solid, stable, easy-to-use standard functions such as microprocessors or microperipherals. These functions allow the designer to concentrate on unique value-added features without re-inventing standard functions. Combining VAutomation megafunctions with other functional blocks and custom logic can produce systems-on-a-chip.

The designer can target VAutomation megafunctions for any architecture, including PLDs, ASICs, gate arrays, or standard cells, and a wide range of operating voltages and fabrication processes. VAutomation AMPP megafunctions are designed to allow prototyping in Altera PLDs and later migration to a custom device in a suitable target architecture.

VAutomation uses strictly synchronous HDL designs with D -flipflops and logic gates that are reliable and easy to synthesize and analyze; feedback loops, multi-cycle paths, latches, and flipflop clear or set pins are not used.

VAutomation megafunctions are available in both VHDL and Verilog HDL source codes. The cores come complete with verification suites and synthesis scripts.

Available Products

VAutomation provides the megafunctions summarized in the following table. Not all products are available for Altera devices. Contact VAutomation for availability.

Megafunction	Description
V6502	High-performance 8-bit microprocessor
VZ80	High-performance 8-bit microprocessor
V8086	Intel-compatible 16-bit microprocessor
V186	Intel/AMD-compatible 16-bit microprocessor
V960	Ethernet LAN controller
V526	High-level data link controller (HDLC)

Altera Sales Offices

February 1997

Altera Regional Offices

NORTHERN CALIFORNIA (CORPORATE HEADQUARTERS)
Altera Corporation
2610 Orchard Parkway
San Jose, CA 95134-2020
TEL: (408) 894-7000
FAX: (408) 433-3943
(408) 894-7755

Altera Corporation
2290 N. First Street, Suite 212
San Jose, CA 95131
TEL: (408) 894-7900
FAX: (408) 894-7979

SOUTHERN CALIFORNIA
Altera Corporation
15375 Barranca Parkway, Suite B-201
Irvine, CA 92618
TEL: (714) 450-0262
FAX: (714) 450-0263

Altera Corporation
Olympic Plaza Executive Center
11500 West Olympic Boulevard, Suite 400
Los Angeles, CA 90064
TEL: (310) 312-4507
FAX: (310) 312-4508

Altera Corporation
5355 Mira Sorrento Place, Suite 100
San Diego, CA 92121
TEL: (619) 597-7518
FAX: (619) 597-7418

ARIZONA
Altera Corporation
2390 E.Camelback Road, Suite 300
Phoenix, Arizona 85016
TEL: (602) 553-1090
FAX: (602) 553-1198

COLORADO
Altera Corporation
Denver Technology Center
7900 East Union Avenue, #1100
Denver, CO 80237
TEL: (303) 694-5352
FAX: (303) 694-5351

Altera Corporation
14142 Denver West Parkway, #200
Golden, CO 80401
TEL: (303) 216-0167
FAX: (303) 277-0429

GEORGIA
Altera Corporation
3675 Crestwood Parkway, Suite 400
Duluth, GA 30136
TEL: (770) 935-6070
FAX: (770) 935-6073

ILLINOIS
Altera Corporation
475 N. Martingale Road, Suite 420
Schaumburg, IL 60173
TEL: (847) 240-0313
FAX: (847) 240-0266

MARYLAND
Altera Corporation
9891 Broken Land Parkway, Suite 300
Columbia, MD 21046
TEL: (410) 312-5708
FAX: (410) 309-0720

MASSACHUSETTS
Altera Corporation
238 Littleton Road, Suite 207
Westford, MA 01886
TEL: (508) 392-1100
FAX: (508) 392-1157

MINNESOTA
Altera Corporation
2850 Metro Drive, Suite 250
Bloomington, MN 55425
TEL: (612) 851-7861
FAX: (612) 858-7258

NEW JERSEY
Altera Corporation
575 State Highway 28
Raritan, NJ 08869
TEL: (908) 526-9400
FAX: (908) 526-5471

NORTH CAROLINA
Altera Corporation
5511 Capital Center Drive, Suite 110
Raleigh, NC 27606
TEL: (919) 852-1004
FAX: (919) 852-0809

OHIO
Altera Corporation
7784 Reynolds Road
Mentor, OH 44060
TEL: (216) 946-8211
FAX: (216) 946-9411

Altera Regional Offices

(Continued)

OREGON
Altera Corporation
11000 S.W. Stratus Street, Suite 330-17
Beaverton, OR 97008
TEL: (503) 643-8447
FAX: (503) 644-2345

TEXAS
Altera Corporation
5080 Spectrum Drive, Suite 812W
Dallas, TX 75248
TEL: (972) 701-2330
FAX: (972) 701-2331

TEXAS *(continued)*
Altera Corporation
9430 Research Boulevard
Echelon IV, Suite 400
Austin, TX 78759
TEL: (512) 343-4542
FAX: (512) 418-1186

CANADA
Altera Corporation
300 March Road, Suite 601B
Kanata, Ontario K2K 2E2
Canada
TEL: (613) 599-3141
FAX: (613) 599-3143

Altera International Sales Offices

UNITED STATES
(CORPORATE HEADQUARTERS)
Altera Corporation
2610 Orchard Parkway
San Jose, CA 95134-2020
USA
TEL: (408) 894-7000
FAX: (408) 433-3943
(408) 894-7755

UNITED KINGDOM
(EUROPEAN HEADQUARTERS)
Altera UK Limited
Holmers Farm Way
High Wycombe
Buckinghamshire
HP12 4XF
United Kingdom
TEL: (44) 1 494 602 000
FAX: (44) 1 494 602 001

NORTHERN EUROPE
Altera UK Limited
Holmers Farm Way
High Wycombe
Buckinghamshire
HP12 4XF
United Kingdom
TEL: (44) 1 494 602 020
FAX: (44) 1 494 602 021

BELGIUM
Altera Belgium
Katwilgweg 7B
2050 Antwerpen
Belgium
TEL: (32) 3 254 0420|
FAX: (32) 3 254 0320

FRANCE
Altera France S.A.R.L.
Le Mermoz
13 Avenue Morane Saulnier
78140 Velizy
France
TEL: (33) 1 34 63 07 50
FAX: (33) 1 34 63 07 51

GERMANY
Altera GmbH
Max-Planck-Str. 5
D-85716 Unterschleissheim
Germany
TEL: (49) 89 3218 250
FAX: (49) 89 3218 2579

HONG KONG
Altera Hong Kong
Suite 1008, Tower 1
China Hong Kong City
33 Canton Road, Tsimshatsui
Kowloon, Hong Kong
TEL: (852) 2377-0218
FAX: (852) 2377-2811

ITALY
Altera Italia S.R.L.
Corso Lombardia 75
Autoporto Pescarito
10099 San Mauro, Torinese (Torino)
Italy
TEL: (39) 11 223 8588
FAX: (39) 11 223 8589

JAPAN
Altera Japan, Ltd.
Shinjuku Mitsui Building 36F
2-1-1, Nishi-Shinjuku
Shinjuku-ku, Tokyo 162-04
Japan
TEL: (81) 3 3340 9480
FAX: (81) 3 3340 9487

KOREA
Altera Korea
Youndang Building, Suite 501
144-23 Samsung-dong, Kangnam-Ku
Seoul, Korea 135-090
TEL: (82) 2 538-6895
FAX: (82) 2 538-6896

SWEDEN
Altera AB
Sjoangsvagen 15
192 72 Sollentuna
Sweden
TEL: (46) 8 626 60 91
FAX: (46) 8 626 60 99

Abbreviations

February 1997

ACIA	Asynchronous communications interface adapter
ADC	Analog-to-digital converter
ADPCM	Adaptive Differential Pulse Code Modulation
AHDL	Altera Hardware Description Language
ALU	Arithmetic logic unit
AM	Amplitude modulation
AMPP	Altera Megafunction Partners Program
ASIC	Application-specific integrated circuit
ASK	Amplitude shift keying
ASPEC	Application-specific processor engine megafunction
ASSP	Application-specific standard product
ATM	Asynchronous Transfer Mode
AWT	Adaptive wavelet transform
BCT	Binary Coded Ternary
BIST	Built-in self test
CAD	Computer-aided design
CCITT	International Telegraph and Telephone Consultation Committee
CODEC	Coder/decoder
CPLD	Complex programmable logic device
CPM	Continuous phase modulation
CPU	Central processing unit
CRC	Cyclic redundancy check
DAB	Digital audio broadcast
DAC	Digital-to-analog converter
DCME	Digital circuit multiplication equipment
DCT	Discrete cosine transform
DDS	Direct digital synthesis
DFT	Discrete Fourier transform
DMA	Direct-memory access
DRAM	Dynamic random access memory
DSP	Digital signal processing
DSS	Digital satellite system
DSSS	Direct sequence spread spectrum
DUT	Device under test
DVB	Digital video broadcast
EAB	Embedded array block
ECC	Error correction coding
ECL	Emitter-coupled design
ECP	Extended capabilities port

EDA	Electronic Design Automation
EEPROM	Electrically erasable programmable read-only memory
EISA	Extended industry-standard architecture
FFT	Fast Fourier transform
FIFO	First-in first-out
FIR	Finite impulse response
FISP	Foundry Independent Standard Product
FLEX	Flexible Logic Element MatriX
FM	Frequency modulation
FSK	Frequency shift keying
GUI	Graphical user interface
HDL	Hardware description language
HDLC	High-level data link controller
IC	Integrated circuit
ICR	In-circuit reconfigurability
IP	Intellectual property
IEEE	Institute of Electrical and Electronic Engineers
IIR	Infinite impulse response
I/O	Input/output
ISA	Industry-standard architecture
ISP	In-system programmability
ITU	International Telegraphy Union
ISDN	Integrated services digital network
JPEG	Joint Photographic Experts Group
LAN	Local-area network
LFSR	Linear feedback shift register
LIFO	Last-in first-out
LUT	Look-up table
MAC	Multiplier-accumulator
MAX	Multiple Array MatriX
MCU	Microcontroller unit
MIDI	Musical instrument digital interface
MOR	Models on request
MPEG	Motion Pictures Expert Group
NCO	Numerically controlled oscillator
OEM	Original equipment manufacturer
PCI	Peripheral component interconnect
PCM	Pulse-code modulation
PCS	Personal communications system
PLD	Programmable logic device
PLL	Phase-locked loop
PN	Pseudo-random number
PPI	Programmable peripheral interface
PSK	Phase shift keying
PVP	Packetized voice protocol
QAM	Quadrature amplitude modulation
QPSK	Quadrature phase shift keying

RAM	Random access memory
RAMDAC	Random access memory digital-to-analog converter
RF	Radio frequency
RISC	Reduced instruction set computing
RLE	Run, length encoding
ROM	Read-only memory
RTL	Register transfer level
SCVL	Standard component VHDL library
SIG	Special interest group
SRAM	Static random access memory
TCM	Trellis coded modulation
TTL	Transistor-to-transistor logic
UART	Universal asynchronous receiver/transmitter
USART	Universal synchronous/asynchronous receiver/transmitter
USB	Universal serial bus
VME	Versa Module Eurocard
VLSI	Very large-scale integration
XMIDI	Extended musical instrument digital interface